HX3009 Data Sheet

1 Product Definition

HX3009 is an ultra-low power integrated proximity sensor for head phone application.

2 Description

HX3009 is an ultra-low power integrated proximity sensor with a built-in IR Laser Diode (LD) and I²C interface in *2×1mm* 6pin package (MSL3). The device is designed for the short distance detection with auto ambient light and structure crosstalk noise cancellation function. **Fig.1** shows the simplified block diagram of the device. Detail information and specification of each function blocks will be described in following sections.

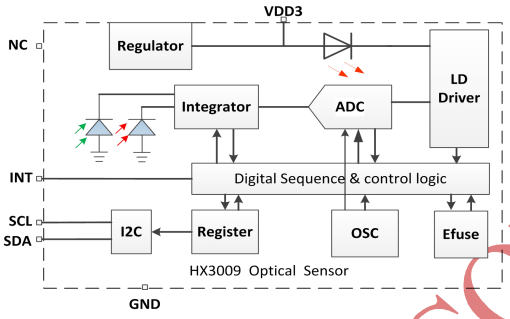

Figure 1. Simplified Block Diagram

3 Features

- **Proximity Sensing:**

1. Ultra low power design:
   Normal mode: 20*μA*
   @ PWT = 400ms , LD on time = *512μs*, LD driver = *12.5mA*.
   Sleep mode: less than ***0.1 μA***.
2. Auto cancellation of structure crosstalk.
3. Also has built-in Offset DAC for manual structure crosstalk cancellation and the max cancellation range can be *100X* to the signal current.
4. Auto ambient light suppression up to 100k Lux.
5. Also supports digital ambient light cancellation.
6. Auto compensation of LD and PD temp variation.
7. I²C address software re configurable. Master device can drive two HX3009 through the same I²C bus line.
8. Auto proximity sensing immediately after power on without master control.
9. Intelligent detection scheme to reduce false interrupt.

- **Transmitter:**

1. Built-in 940*nm* Infrared Red Laser Diode.
2. Programmed low noise IR-LD current driver: 6.25/9.375/12.5/18.75/25/37.5/50/75 *mA*.
3. Programmable LD on-time: 16*μs*-1024*μs*.
4. Ultra low average current: less than 15*μA*.

- **Receiver:**

1. *10-16* bits ADC output for proximity detection.
2. Auto ambient light suppression up to 65*dB* under 100*k* Lux light intensity.
3. Built-in Offset DAC to cancel structure induced crosstalk light as high as *100x* useful IR light induced photodiode current.
4. PGA gain programmable: *1x-16x*.
5. Ultra low power consumption: less than 7*μA*.

- **Sensing Waiting Time Selectable: 1 ms to 1600 ms**
- **Operating Temperature: -30℃ to 85℃**
- **Power Supply: Single 2.9V~3.6V**
- **I²C Bus Voltage: 1.7V-2V**
- **Supports I²C Interface up to 400kHz**
- **Supports Single-Master-Two-Slave Application**

4 Applications

Smart Phone, PAD
Head Phone, Smart Wearable

5 Package Information

***2×1×0.5mm*, OLGA-6**

Content

6 Pin Configuration

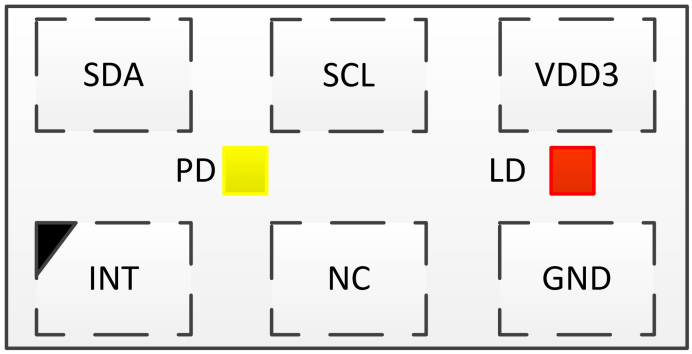

Figure 2. HX3009 Top View

TABLE I. HX3009 PIN LIST

PIN	NAME	TYPE	DESCRIPTION
1	INT	D	Interrupt signal (OD and CMOS selectable)
2	NC		
3	GND	Ground	Power Ground
4	VDD3	Power	Anode of Laser diode and Power supply of IC
5	SCL	D	I^2C CLK, external pull up resistor (recommended10kΩ for 400KHz)
6	SDA	D	I^2C data, external pull up resistor (recommended10kΩ for 400KHz)

7 Specifications

7.1 Absolute Maximum Rating (T_a=25℃, unless otherwise specified)

TABLE II. HX3009 ABSOLUTE MAXIMUM RATING

PARAMETER	MIN	MAX	UNIT
VDD to GND	-0.3	3.6	V
Analog inputs	GND – 0.3	VDD + 0.3	V
Digital inputs	GND – 0.3	VDD + 0.3	V
Input current to any pin except supply pins		±7	mA
Operating temperature range	-30	85	℃
Maximum junction temperature		125	℃

7.2 Recommended Operating Conditions

TABLE III. HX3009 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
VDD	2.9	3.6	V
Supply voltage accuracy	±5		%
Specified temperature range	-30	85	℃
Maximum junction temperature		125	℃

7.3 ESD Ratings

TABLE IV. HX3009 ESD RATINGS

		VALUE	UNIT
V(ESD) Electro-Static Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±250	

7.4 Electrical Characteristics

Typical specifications are at *25°C*, *VDD = 3.3V*, *VBUS = 1.8V*, *PWT = 400ms*, LD driver current = *12.5mA*, LD on-time = *512µs*, *32kHz* and *1MHz* internal clock, unless otherwise noted.

TABLE V. HX3009 ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROXIMITY SENSING9					
Power Consumption	Normal mode @PWT = 100*ms*, LD Current = 12.5*mA*		***65***	***90***	*µA*
	Sleep mode			***0.1***	*µA*
	Standby mode			***7***	*µA*
Ambient Light Suppression	@ 100K Lux light density	***65***(1)			*dB*
PS Dark Code	@OSR=4096			***1.5***(1)	*%FS*
	@OSR=65536			***1.5***(1)	*%FS*
PS Waiting Time (PWT)	Default Value		***200***		*ms*
PS Waiting Time Range	Selectable		**1/2/3/4/5/6/ 7/8/25/50/1 00/200/400/ 800/1600**		*ms*
RECEIVER					
Offset iDAC Current Range	4 bits iDAC		**5/10/..../70/ 75** (1)		*nA*
Offset iDAC Current Step			**5** (1)		*nA*
PGA Gain	Default Value		**8** (1)		
PGA Gain Setting	4 bits Control, Selectable		**1/2/...../15/ 16** (1)		
ADC Resolution	Default Value		**12** (1)		*Bit*
ADC Resolution Range	3 bits Control, Selectable(0-4)		**10/12/13/14 /16** (1)		*Bit*
ADC iDACn Current	Default Value		**800**		*nA*
ADC iDACn Current Range	3 bits control, Selectable		**100/200/.../1 500/1600** (1)		*nA*
TRANSMITTER					
LD Current Range	3 bits control		**6.25/9.375/1 2.5/18.75/25 /37.5/50/75** (1)		*mA*
CLK (Internal *32kHz* Oscillator)					
Frequency			***32***		*kHz*
Accuracy	Room temperature	***-10%***		***+10%***	
I²C INTERFACE					
Maximum Clock Speed			***400***		*kHz*
I²C Slave Address			**0x44**		
I²C Slave Address(1-Master to2-Slaves)			**0x44 and 0x45**(1)		
DIGITAL INPUTS					
V_{IH}, High-level input voltage		***0.7*Vbus***			*V*
V_{IL}, Low-level input voltage				***0.3*Vbus***	*V*
DIGITAL OUTPUTS					
V_{OH}, High-level output voltage			***Vbus***		*V*
V_{OL}, Low-level output voltage			***0***		*V*

Notes:

1: **Guarantee by characterization**

8 Detailed Description

8.1 Overview

HX3009 is an ultra-low power integrated proximity sensor with a built-in IR Laser Diode (LD) and I²C interface in *2×1mm* 6pin package (MSL3). It incorporates a Photo-Diode (PD), Programmable Gain Amplifier (PGA), an Offset Current DAC (iDAC), System Oscillator (OSC*32kHz*), Digital Timing Controller (OSC*1MHz*) and ADC Block in the same chip and also incorporates an Infrared Red Laser Diode (IR-LD) and built-in Laser Driver with excellent driving performance. The photodiode spectral response is optimized for wavelength *940nm* infrared light. HX3009 provides programmable Laser On-Time setting to drive IR-LD and employs noise cancellation scheme to obtain. For short distance detection use, HX3009 supports Auto Detect Function with interrupt output when power on, and no need for master control. The powerful on-chip digital engine can automatically eliminate the crosstalk light induced by structural reflection. The maximum structural reflection cancellation range is *100x* to the weak useful IR light current. HX3009 also has excellent Auto Ambient Light Suppression Function, and its suppression ratio can as high as *65dB* under maximum *100k LUX* light intensity. For Single-Master-to-Multi-Slave applications, HX3009 Supports 1-Master-to-2-Slave Mode: Users can dynamically reconfigure one HX3009's I²C address to 0x45 and keep the other one to originally 0x44, thus the master can communicate with the two devices simultaneously through the same I²C Bus line.

8.2 Digital State Machine Diagram

HX3009 has mainly three operation modes:

1. **Sleep Mode**
   Which is configured by Power-down (PD) register. All the circuits except I²C are shut down and the power consumption is less than *0.1μA*.
2. **Normal Mode** (including **Prox Check** and **Prox ADC**)
   All the circuits are working to perform proximity sensing.
3. **Standby Mode (PRF Wait)**
   All the circuits except I²C and OSC *32kHz* clock are shut down to save power.

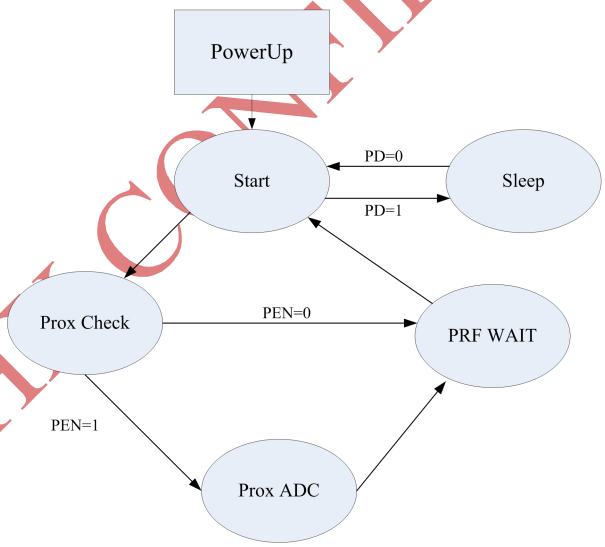

Figure 3. State Machine Diagram

8.3 Timing Diagram

The timing information of HX3009 is as following. The device works under two internal clocks: *32kHz* system clock DCLK32K and *1MHz* ADC timing clock CLK1M. The *32kHz* clock is running all the time unless in chip **sleep mode**. It generates the waiting time configured by register **0x01**. The *1MHz* high frequency clock only enabled in **normal mode**, and used to provide timing source for ADC and other high clock circuits.

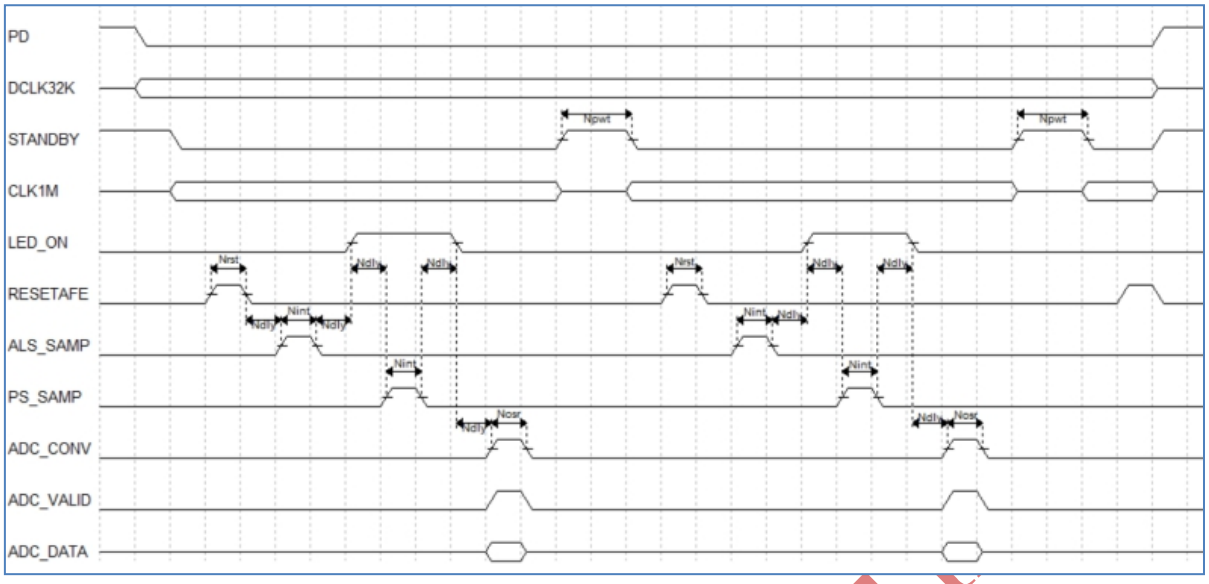

Figure 4. Main Timing Diagram

8.4 ADC Data conversion state Timing Setting (base on *1MHz* clock)

RESETAFE: register 0x02, selectable in 511, 1023, 2047, 4095 No. of Tclk1mhz, recommend 511* $T_{clk1MHz}$;
PS_SAMP: register 0x03<6:4>, selectable in 64, 128, 256,512, 1024, 2048, 4096 No. of $T_{clk1MHz}$, recommend 1024*$T_{clk1MHz}$;
ALS_SAMP: register 0x03<2:0>, selectable in 64, 128, 256,512, 1024, 2048, 4096 No. of $T_{clk1MHz}$, recommend 1024*$T_{clk1MHz}$;
ADC_CONV: register 0x01<2:0>, selectable in 1024, 2048, 4096, 8192, 16384, 32768, 65535 No. of $T_{clk1MHz}$, recommend 4096* $T_{clk1MHz}$;

8.5 Offset IDAC

The Built-in Offset Current DAC (iDAC) can cancel the crosstalk light induced by structural imperfection, and the cancellation ratio can be 100x to the useful photodiode current. The Offset iDAC current range is selectable from *5nA* to *75nA*, and is controlled by registers **--0x13 bit<3:0>**.

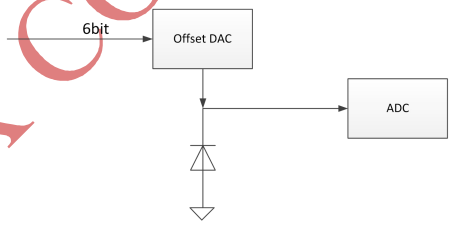

Figure 5. Offset iDAC

8.6 LD Driver

The device has one internal current DAC with 3bits output range control. The DAC output range is controlled through register **0x20 bits<6:4>** (*000 = 6.25 mA*, *001 = 9.375 mA*, *010 = 12.5mA*, *011 = 18.75mA*)

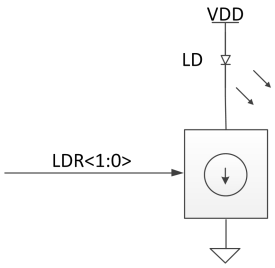

Figure 6. LD driver circuit

8.7 Analog-to-Digital Converter (ADC)

The receiver path has a high precision sigma-delta ADC that provides a largest 16-bit representation of the current from the photodiode. The ADC has configurable over sampling ratio (OSR) set by register **0x01 bit<2:0>**. The ADC output code corresponding to the photodiode current can be read out from two 16-bit registers (**0X07~0X08**) in unipolar straight binary format. The default ADC full-scale input range is *100nA* and the default PGA Gain is *8x*. The mapping of the ADC input current to the ADC output code is shown in the table below.

TABLE VI. ADC OVER SAMPLE RATE = 4095

INPUT CURRENT AT ADC INPUT	*12-BIT ADC OUTPUT CODE(BINARY)*	*16-BIT ADC OUTPUT CODE(DECIMAL)*
0	0000_0000_0000_0000	0
800nA	0000_1111_1111_1111	4095

TABLE VII. ADC OVER SAMPLE RATE = 65535

INPUT CURRENT AT ADC INPUT	*16-BIT ADC OUTPUT CODE(BINARY)*	*16-BIT ADC OUTPUT CODE(DECIMAL)*
0	0000_0000_0000_0000	0
800nA	1111_1111_1111_1111	65535

8.8 I²C Address Software Selectable

For Single-Master-to-Multi-Slave application, HX3009 Supports 1-Master-to-2-Slave Mode: No extra pin or resistor needed, through I²C commands, Users can dynamically switch one HX3009's I²C address to 0x45 while keep the other to originally 0x44, thus the master can communicate with the two devices simultaneously through the same I²C Bus line.

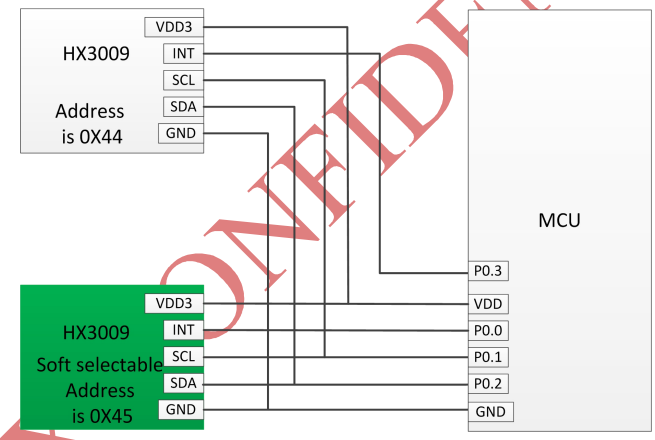

Figure 7. I²C Address Software Selectable

The default addresses of HX3009 is 0X44, Users can Change the device Address from 0X44 to 0X45, before the address change operation, make sure the I²C interface SCL and SDA is connected correctly.

- Step1: Set the INT pin into OD mode, recommend write reg 0x00 with 0x04;
- Step2: Read register 0xA5;
- step3: Configure the MCU pin which connected with INT that you want to change address to Output, and out put low voltage;
- step4: Read register 0xA6;
- step5: Release the MCU pin that connected with INT pin to input and this operation can release the INT pin from keeping low;
- step6: Read register 0x45, to make sure that the address change operation work, if not response, repeat step1 to step 5;

8.9 Auto Structural Crosstalk Light Cancellation

HX3009 has built-in auto structure crosstalk light cancellation function. Its work flow is drawn bellow. The powerful on-chip digital engine can automatically eliminate the crosstalk induced by the structural reflection. And maximum cancellation range can be *100x* to the weak useful signal current.

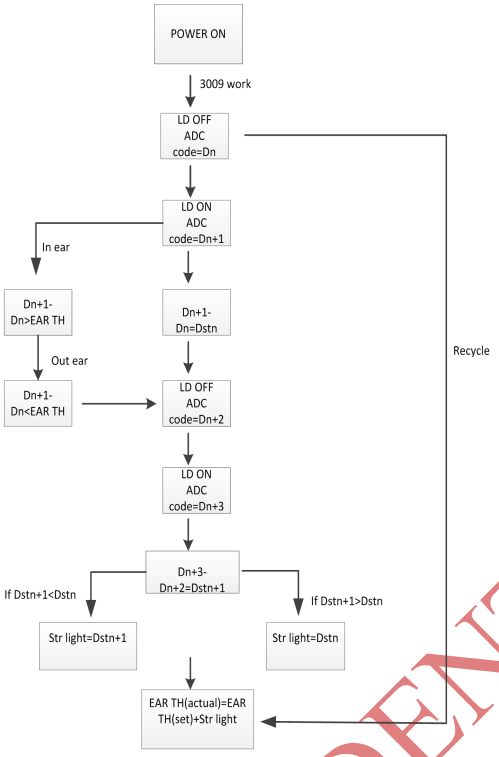

Figure 8. Structure Crosstalk Light Cancellation Work Flow

8.10 Intelligent Interrupt Detection

HX3009 includes two Interrupt mode, CMOS Mode and Open Drain (OD) Mode (INT pin output):

1) CMOS Mode Interrupt Output

This is the default interrupt output mode, and is represented simply by voltage level at IN pin (toggle mode):

A: high voltage when ADC Code is higher than high threshold value

B: low voltage when ADC code is lower than low threshold value

2) OD Mode Interrupt Output

Open Drain (OD) Modeis set by setting the register 0x00 bit<2>，and the definition of voltage level is the same as CMOS mode:

A: high voltage when ADC Code is higher than high threshold value

B: low voltage when ADC code is lower than low threshold value

Both CMOS mode and OD mode, User can also change the interrupt type from toggle mode to I^2C clear mode by setting register 0x00 bit<3>. In I^2C clear mode, by default, INT pin outputs high voltage. Once triggering interrupt, INT pin outputs low voltage and host processor can clear the interrupt by reading ADC data registers.

3) Intelligent Interrupt Detection

HX3009 incorporates an intelligent detection-interrupt scheme to achieve both fast response and low power. After power-on, by default, HX3009 is in slow response mode (long PS waiting time ~*400ms*) for low power. Once detecting a change of input signal and the ADC Code is lower than low threshold (in-ear state) or higher than high threshold (out-ear state), HX3009 adjusts PS waiting time to about *25ms* to speed up the checking of input signal. After accumulating a preset count (for example 1, 4, 8 or 16) of consistent under or over threshold condition, HX3009 triggers the interrupt to report to host processor. If the triggering condition is not met, HX3009 resumes the long waiting time (default 200ms) and goes back to low power mode. This scheme can significantly reduce the false interrupt while still maintaining very low power consumption.

4) INT Trigger Condition Illustration

Count number to trigger the interrupt is set to 4.

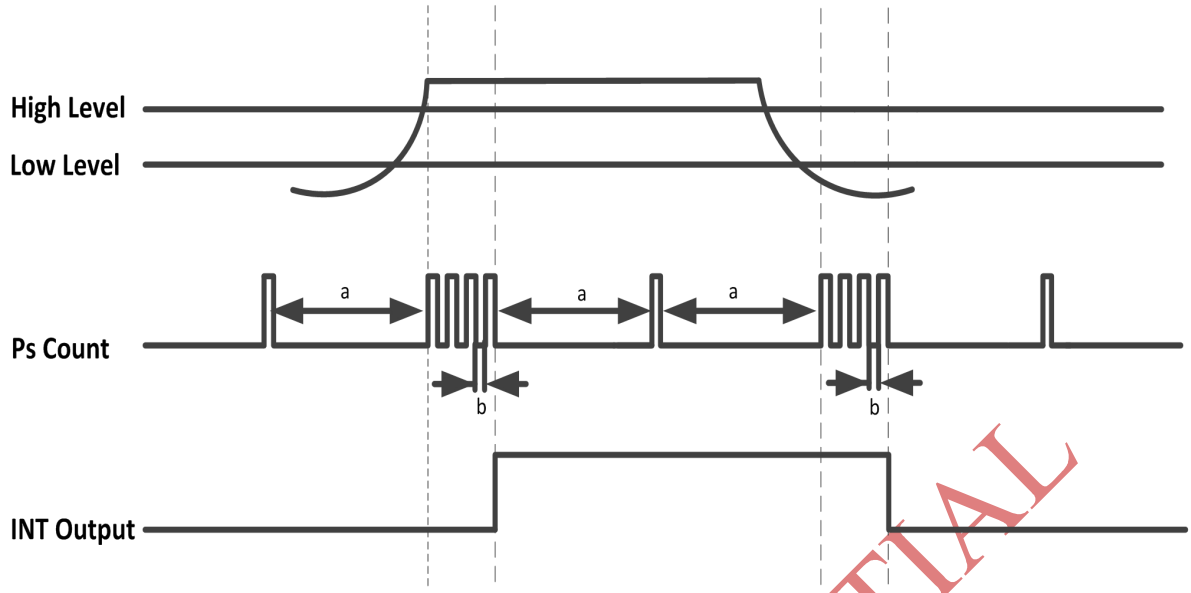

Figure 9. Intelligent Interrupt Scheme

Note:

a: PWT = 400ms

b: PWT= 25ms

9 Register Map

TABLE VIII. REGISTER MAP, ADDR=0X00

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT (BIT)	DESCRIPTION
0x00	RW	0x0A	RESERVED	7:4		
			INT_GEN_MODE_I²C	3	1	1'h0: normal (I²C clear) 1'h1: voltage toggle
			INT MODE	2	0	1'h0: cmos voltage level 1'h1: open-drain
			PEN	1	1	Enable PEN
			PD	0	0	Enable POWER DOWN

TABLE IX. REGISTER MAP, ADDR=0X01

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT (BIT)	DESCRIPTION
0x01	RW	0xC9	WAIT_NUM_I²C	7:4	1100	Wait time 4'h0: wait_time = 0ms 4'h1: wait_time = 1ms 4'h2: wait_time = 2ms 4'h3: wait_time = 3ms 4'h4: wait_time = 4ms 4'h5: wait_time = 5ms 4'h6: wait_time = 6ms 4'h7: wait_time = 7ms 4'h8: wait_time = 8ms 4'h9: wait_time = 25ms 4'hA: wait_time = 50ms 4'hB: wait_time = 100ms 4'hC: wait_time = 200ms 4'hD: wait_time = 400ms 4'hE: wait_time = 800ms 4'hF: wait_time = 1600ms Default = 200ms
			IS_EFUSE_I²C	3	1	Thod value select 1'h0: register 1'h1: efuse
			OSR_NUM_I²C	2:0	001	3'h0: 1024 3'h1: 4096 3'h2: 8192 3'h3: 16384 3'h4: 65535

TABLE X. REGISTER MAP, ADDR=0X02

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X02	RW	0X10	TH_HIGH_I²C[9:8]	7:6	00	High threshold 2 bit MSB
			INT_NUM_I²C	5:4	01	Set interrupt trigger number 2'h0: 1; 2'h1: 2; 2'h2: 4; 2'h3: 7;
			STR_MANU_EN_I²C	3	0	Manual Ambient light cancel enable: 1'h0: Enable 1'h1: Disable
			RESETAFE_NUM_I²C	2	0	Clock Width of RESETAFE 1'h0: 511μs; 1'h1: 1023μs;
			FSM_DELAY_NUM_I²C	1:0	00	Clock Width of DELAY 2'h0: 4μs; 2'h1: 5μs; 2'h2: 6μs; 2'h3: 7μs;

TABLE XI. REGISTER MAP, ADDR=0X03

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X03	RW	0X66	EFUSE_CLK_EN	7	0	Enable of efuse clock 1'h0: No 1'h1: Yes;
			PS_SAMP_NUM_I²C	6:4	110	Clock Width of PS Sample 3'h0: 0μs 3'h1: 16μs 3'h2: 32μs 3'h3: 64μs 3'h4: 128μs 3'h5: 256μs 3'h6: 512μs 3'h7: 1024μs
			ALS_TEST	3	0	Enable Only ALS function 1'h0: disable 1'h1: enable
			ALS_SAMP_NUM_I²C	2:0	110	Clock Width of ALS Sample 3'h0: 0μs 3'h1: 16μs 3'h2: 32μs 3'h3: 64μs 3'h4: 128μs 3'h5: 256μs 3'h6: 512μs 3'h7: 1024μs

TABLE XII. REGISTER MAP, ADDR=0X04,0X05

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X04	RW	0x64	TH_HIGH_I²C[11:4]	7:0	0110 0100	High threshold mid 8b, discard low 4b
0X05	RW	0x25	TH_LOW_I²C[11:4]	7:0	0010 0101	Low threshold mid 8b, discard low 4b

TABLE XIII. REGISTER MAP, ADDR=0X06

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X06	RW	0X51	STR_SEL	7:6	01	Set first sample time of str data 2'h0: STR_SEL = 'd1; 2'h1: STR_SEL = 'd4; 2'h2: STR_SEL = 'd8; 2'h3: STR_SEL = 'd15;
			LDON_SEL	5:4	01	LD control type 2'h0: LD ON every cycle 2'h1: LD ON/OFF interleave 2'h2: LD OFF 2'h3: LD ON DC CUR TEST
			AVG_EN	3	0	Enable of Data average 1'h0: Do not Average 1'h1: Do Average
			SAMP_CYCLE	2:0	001	Set number of cycle in PRF 3'h0: 1 3'h1: 2 3'h2: 4 3'h3: 8 3'h4: 16 3'h5: 32 3'h6: 64

TABLE XIV. REGISTER MAP, ADDR=0X07,0X08

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X07	RO	0x64	ADC_DATA[7:0]	7:0		ADC raw data low 8bit
0X08	RO	0x25	ADC_DATA[15:8]	7:0		ADC raw data high 8bit

TABLE XV. REGISTER MAP, ADDR=0X09

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X09	RO		RESERVED	7:1		
			INT_FLAG	0		Int flag 1'h0: Lower than T_{HODL} 1'h1: Higher than T_{HODH}

TABLE XVI. REGISTER MAP, ADDR=0X10~0X13

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X10	RW	0xA0	STR_SELF_EN	7	1	Self str cancel enable
			HALF_EN	6	0	Enable of thod halve
			LEDCUR<5:0>	5:0	100000	Trim bit of led bias current
0x11	RW	0x77	ADC_DACN	7:4	0111	ADC Range Select
			OSCBIAS	3:0	0111	OSC32K Freq Triming
0x12	RW	0xF4	IPD_PGA	7:4	1111	PGA Gain
			RESERVED	3		
			THODH	2:0	100	High threshold select
0x13	RW	0x20	FLAG	7	0	Efuse burn flag
			THODL	6:4	010	Low threshold select
			OFFSET_DAC	3:0	000	Offset DAC

TABLE XVII. REGISTER MAP, ADDR=0X14~0X16

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X14	RW	0x45	PWE_PULSE_CYCLE_I²C<7:0>	7:0	01000101	Pulse width of effuse burn bit<7:0>
0x15	RW	0x01	RESERVED	7:3		
			EFFUSE_PROG_CONFIRM0/1	2	0	Digital func check
			IS_READ_DATA	1	0	Data ready int or ear in/out int select
			PWE_PULSE_CYCLE_I²C<8>	0	1	Pulse width of effuse burn bit<8>
0x16	RW	0x00	RESERVED	7		
			OPEN_VPP	6	0	Enable int to OD input mode
			EFUSE2ADC_SEL	5	0	Read efuse or reg value to dig 1'h0: effuse 1'h1: reg write
			RESERVED	4:0		

TABLE XVIII. REGISTER MAP, ADDR=0X20

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X20	RW	0X28	FREQTEST	7	0	OSC32K Temp Control
			LEDDR<2:0>	6:4	010	LD current output level 3'h0: 6.25mA 3'h1: 9.375mA 3'h2: 12.5mA 3'h3: 18.75mA 3'h4: 25mA 3'h5: 37.5mA 3'h6: 50mA 3'h7: 75mA
			OSC1MTRIM	3:0	1000	OSC2M Freq Trim

TABLE XIX. REGISTER MAP, ADDR=0X21

ADDRESS	TYPE	DEFAULT	NAME	BIT	DEFAULT	DESCRIPTION
0X21	RW	0X53	IRPDSEL<1>	7	0	ALS /IR PD Select 1'h0: do not sel ALS PD 1'h1: sel ALS PD
			IRPDSEL<0>	6	1	ALS SAMPLE Reset 1'h0: always reset not ALS phase 1'h1: normal work with ALS phase
			I1P8SEL	5	0	1.8V IO Torrance Select

						defaults=0
			CKDIVSEL	4	1	OSC_2M_core output choose, 1'h0: div1； 1'h1: div2；output 1MHz
			RESERVED	3:2		
			OSCTEST<1:0>	1:0	11	OSC Test; 2'h0: PDON_RST 2'h1: DCLK32K 2'h2: MCLK1M 2'h3: INT Output

10 Digital Interface

10.1 I²C

10.1.1 I²C Data format

The I²C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The7-bit device addresses 0x44. The register index will automatically increase by after the addresses register has been accessed (read or write). And the format is shown as following:

- Master-to-Slave
- Slave-to-Master

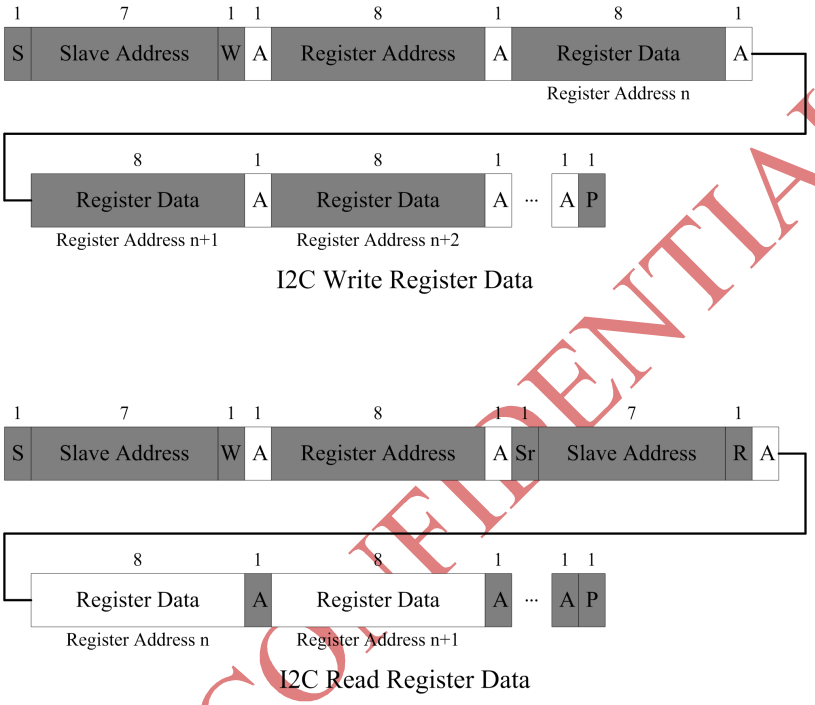

Figure 10. I²C Data Format Diagram

Note:

A: Acknowledge (0)

P: Stop Condition

R: Read (1)

S: Start Condition

W: Write (0)

Sr: Repeated Start Condition

10.1.2 I²C AC Timing

TABLE XX. CHARACTERISTICS OF THE SDA AND SCL I/O STAGES FOR F/S-MODE I²C-BUS DEVICES

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 -0.5 -0.5	 1.5 $0.3V_{DD}$	 n/a -0.5	 n/a $0.3V_{DD}$ (1)	 *V* *V*
High level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 (2) (2)	 n/a $0.7V_{DD}$ (1)	 n/a (2)	 *V* *V*
Hysteresis of Schmitt trigger inputs: VDD > *2V* VDD < *2V*	V_{hys}	 n/a n/a	 n/a n/a	 $0.05V_{DD}$ $0.1V_{DD}$	 –	 *V* *V*
LOW level output voltage (open drain or open collector) at 3 *mA* sink current: V_{DD} > *2V* V_{DD} < *2V*	V_{OL1} V_{OL3}	 0 n/a	 0.4 n/a	 0 0	 0.4 $0.2V_{DD}$	 *V* *V*
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 *pF* to 400 *pF*	t_{of}	–	250(4)	$20 + 0.1C_b$(3)	250(4)	*ns*
Pulse width of spikes which must be suppressed by the input filter	t_{sp}	n/a	n/a	0	50	*ns*
Input current each I/O pin with an input voltage between 0.1 V_{DD} and 0.9 $V_{DD\,max}$	I_i	-10	10	-10(5)	10(5)	*mA*
Capacitance for each I/O pin	C_i	-	10	-	10	*pF*

Notes:

1. Devices that use non-standard supply voltage switch don't conform to the intended I²C-bus system levels must relate input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5V$.
3. C_b = capacitance of one bus line in *pF*.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table2 (*300ns*) is longer than the specified maximum t_{of}
5. For the output stages (*250ns*). This allows series protection resistors (R_S) to be connected between the SDA/SCL
6. Pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
7. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
8. n/a = not applicable

TABLE XXI. CHARACTERISTICS OF THE SDA AND SCL BUS LINES FOR F/S-MODE I²C-BUS DEVICES

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	*kHz*
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	–	0.6	n/a	*µs*
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	*µs*
HIGH period of the SCL clock	t_{HIGH}	4	–	0.6	–	*µs*
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	*µs*
Data hold time	$t_{HD;DAT}$	0[9]	3.45[10]	0	0.9[10]	*µs*
Data set-up time	$t_{SU;DAT}$	250	n/a	100[11]	–	*ns*
Rise time of both SDA and SCL signals	t_r	–	1000	20 + 0.1C_b[12]	300	*ns*
Fall time of both SDA and SCL signals	t_f	–	300	20 + 0.1C_b[12]	300	*ns*
Set-up time for STOP condition	$t_{SU;STO}$	4	–	0.6	–	*µs*
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	*µs*
Capacitive load for each bus line	C_b	–	400	–	400	*pF*
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	*0.1V_{DD}*	–	0.1V_{DD}	–	*V*
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	*0.2V_{DD}*	–	0.2V_{DD}	–	*V*

Notes:

9. All values referred to V_{IHmin} and V_{ILmax} levels (see Table1).
10. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ min}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
11. The maximum $T_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (T_{LOW}) of the SCL signal.
12. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the require meant $T_{SU;DAT}$ 250ns must the be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such advice does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.
13. t_{rmax} +$t_{SU;DAT}$ = *1000 + 250 = 1250 ns* (according to the Standard-mode I²C-bus specification) before the SCL line is released.
14. C_b = total capacitance of one bus line in *pF*. If mixed with HS-mode devices, faster fall-times according to Table6 are allowed.
15. n/a = not applicable

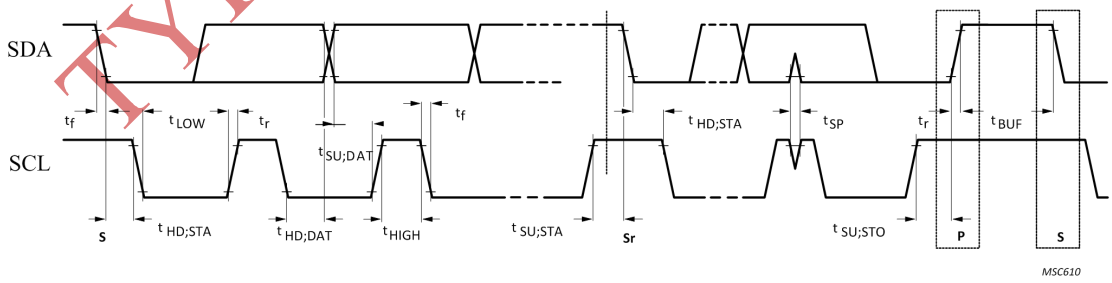

Figure 11. I²C Timing Diagram

11 Application Information

Typical application for HX3009 is showing below:

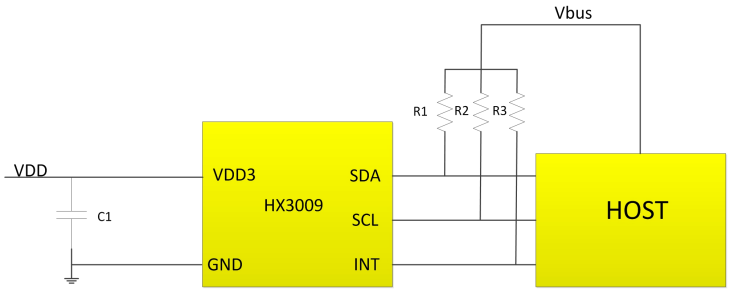

Figure 12. Typical Application Schematic

And the device value is listed below:

TABLE XXII. DEVICE VALUE

DEVICE NAME	*VALUE*	*DESCRIPTION*
V_{DD}	*2.9~3.6 V*	Low noise
V_{bus}	*1.7~2V*	
C1	*1μF*	
R1	*10 KΩ*	
R2	*10 KΩ*	
R3	*10 KΩ*	

12 Package Information

Unit: ***mm***

Body size Tolerance: ±**0.075**

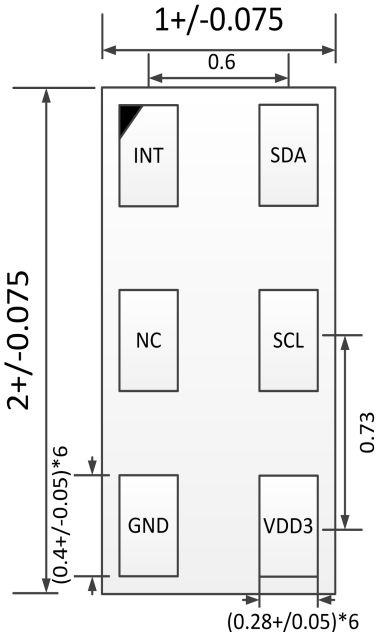

Figure 13. Package Top View

Figure 14. Package Side View

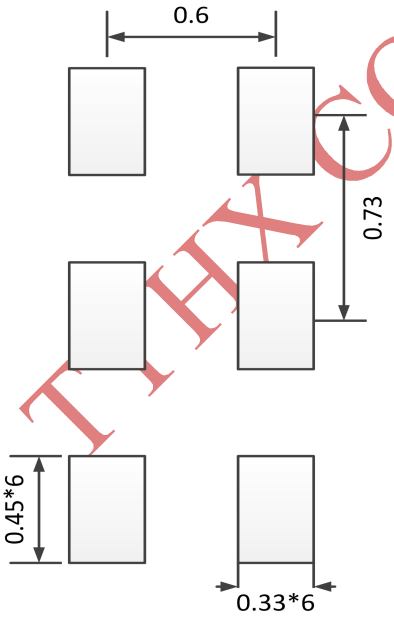

Figure 15. PCB Land Pattern View

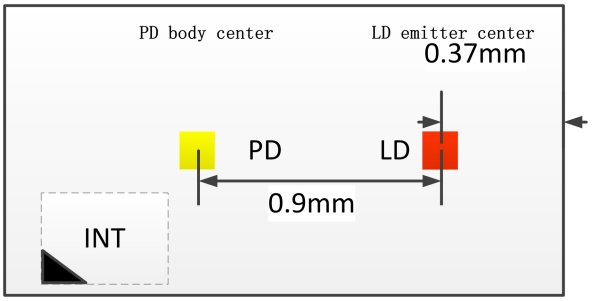

Figure 16. Optical View

13 Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate, the process, equipment material used in these tests are detailed below, the solder reflow profile describes the expect maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

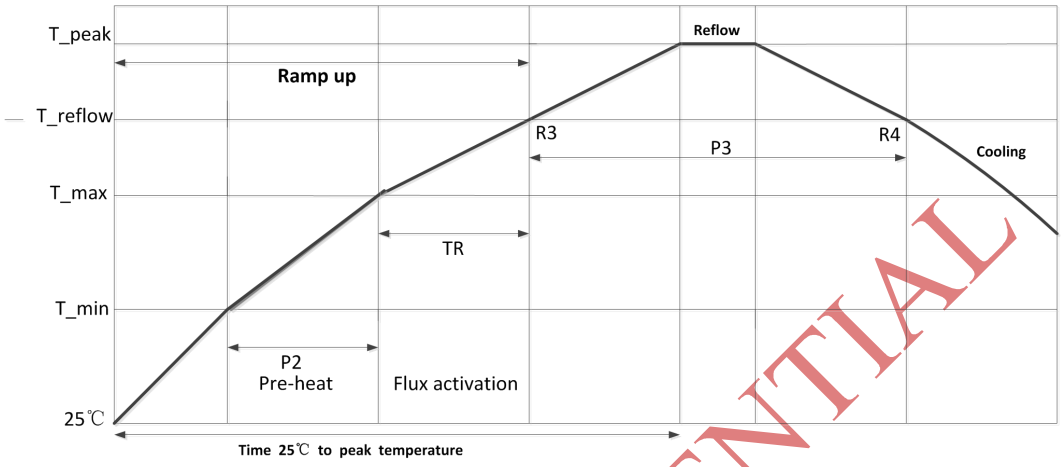

Figure 17. Solder Reflow Profile Grape

TABLE XXIII. SOLDER REFLOW PROFILE

	PEAK TEMPERATURE (T_{PEAK})	***250-255 ℃; MAX 5SEC***
Pre-Heat	Temperature min (T_{min})	150℃; 2℃/Sec
	Temperature max (T_{max})	150-217℃； 100*s* to *180s*
	P2:(T min to max)	90-110*s*
Time maintain above	Temperature (Treflow)	217℃
	Time (P3)	60-90 sec
	R3 Slope (from 217℃ to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	*480s* Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

Change List			
V1.0	Initial	Tom zhao	2020.01.09
V2.0	Added tolerance of Body size	Tom.zhao	2021.04.19