HX3002 Data Sheet

1 Product Definition

HX3002 is an ultra-low power integrated proximity sensor for head phone application.

2 Description

HX3002 is an ultra-low power integrated proximity sensor with a built-in IR Laser Diode (LD) and I2C interface in 2×1.6mm 6pin package (MSL3). The device is designed for the short distance detection with auto ambient light and structure crosstalk noise cancellation function.

3 Features

Proximity Sensing:

1. Ultra low power design:
   normal mode: 20uA@ PWT=400ms，
       LD on time = 512us, LD driver = 12.5mA.
   sleep mode: less than 0.1 μA.
2. Auto cancellation of structure crosstalk
3. Also has built-in Offset DAC for manual structure crosstalk cancellation and the max cancellation range can be 100X to the signal current.
4. Auto ambient light suppression up to 100kLux.
5. Also supports digital ambient light cancellation
6. Auto compensation of LD and PD temp. variation
7. I2C address software re configurable. Master device can drive two HX3002 through the same I2C bus line.
8. Intelligent detection scheme to reduce false interrupt.

Transmitter:

1. Built-in 940nm Infrared Red Laser Diode.
2. Programmed low noise IR-LD current driver: 6.25/9.375/12.5/18.75mA.
3. Programmable LD on-time: 64us-4096us.
4. Ultra low average current: less than 15uA.

Receiver:

1. 10-16 bits ADC output for proximity detection
2. Auto ambient light suppression up to 65dB under 100kLux light intensity.
3. Built-in Offset DAC to cancel structure induced crosstalk light as high as 100x useful IR light induced photodiode current.
4. PGA gain programmable: 1X-16X.
5. Ultra low power consumption: less than 5uA.

Sensing Waiting Time Selectable: 25ms to 1600ms
Supports I2C Interface up to 400KHz
Supports Single-Master-Two-Slave Application
Operating Temperature: -20℃ to 85℃
**Power Supply: Single 2.9V~3.6V**
I2C bus voltage: 1.7V~VDD

4 Applications

Smart Phone, PAD
Head Phone, Smart Wearable

5 Package Information

2×1.6×0.7mm, OLGA-6
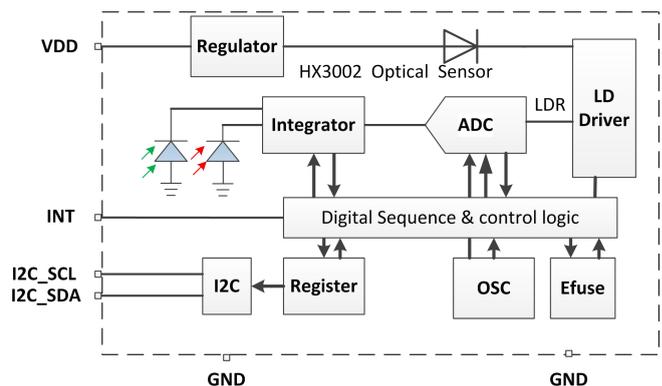
Simplified Block Diagram

Content

6 Pin Configuration

Figure 6.1. HX3002 Top View

6.1 Pin List

Pin	Name	Type	Description
1	VDD	P	Power supply
2	SCL	D	I2C CLK,needs external pull up resistor (for example, 10 kΩ)
3	GND	P	GND
4	GND	P	GND
5	INT	D	Interrupt PIN (OD and CMOS)
6	SDA	D	I2C data,needs external pull up resistor (for example, 10 kΩ)

7 Specifications

7.1 Absolute Maximum Rating(T_a=25℃,unless otherwise specified)

Parameter	Min	Max	Unit
VDD to GND	-0.3	3.6	V
Analog inputs	GND − 0.3	VDD + 0.3	V
Digital inputs	GND − 0.3	VDD + 0.3	V
Input current to any pin except supply pins		±7	mA
Operating temperature range	-20	85	℃
Maximum junction temperature		125	℃

7.2 Recommended Operating Conditions

	Min	Max	Unit
VDD	2.9	3.6	V
Supply voltage accuracy	±5		%
Specified temperature range	-20	85	℃
Maximum junction temperature		125	℃

7.3 ESD Ratings

		Value	Unit
V(ESD) Electro-Static Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±250	

7.4 Electrical Characteristics

Typical specifications are at 25°C,VDD=3.3V, PWT=400ms, LD driver current=12.5mA,LD on-time=512us, 32KHz and 1MHz internal clock, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROXIMITY SENSING					
Power Consumption	Normal mode @PWT=400ms, LD Current=12.5mA		20	25	uA
	Sleep mode			0.1	uA
	Standby mode			7	uA
Ambient Light Suppression	@ 100K Lux light density		65[1]		dB
PS Dark Code	@OSR=4096			2.5[1]	%FS
	@OSR=65536			2.5[1]	%FS
PS Waiting Time (PWT)	Default Value		400		ms
PS Waiting Time Range	Selectable		25/50/100/200/400/800/1600		ms
RECEIVER					
Offset iDAC Current Range	6 bits iDAC	12.5		800	nA
Offset iDAC Current Step			12.5[1]		nA
PGA Gain	Default Value		8[1]		
PGA Gain Setting	4 bits Control, Selectable		1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16		
ADC Resolution	Default Value		12		Bit
ADC Resolution Range	3 bits Control, Selectable		10/11/12/13/14/15/16		Bit
ADC iDACn Current	Default Value		800		nA
ADC iDACn Current Range	3 bits control, Selectable		100/200/.../1500/1600 [1]		nA
TRANSMITTER					
LD Current Range	2 bits control		6.25/9.375/12.5/18.75[1]		mA
CLK (Internal 32KHz Oscillator)					
Frequency			32		KHz
Accuracy	Room temperature		±10%		
I2C INTERFACE					
Maximum Clock Speed			400		KHz
I2C Slave Address			0x44		
I2C Slave Address(1-Master to2-Slaves)			0x44 and 0x45[2]		
DIGITAL INPUTS					
V_{IH} High-level input voltage		0.7*Vbus			V
V_{IL} Low-level input voltage				0.3*Vbus	V
DIGITAL OUTPUTS					
V_{OH} High-level outputvoltage			Vbus		V
V_{OL} Low-level output voltage			0		V

Notes:

1: **Guarantee by characterization**

2:**Default 0X44**

7.5 Typical Characteristics

@ T = 25℃, VDD = 3.3V, PWT = 400ms, LD Current = 12.5mA, LD on time = 512us.
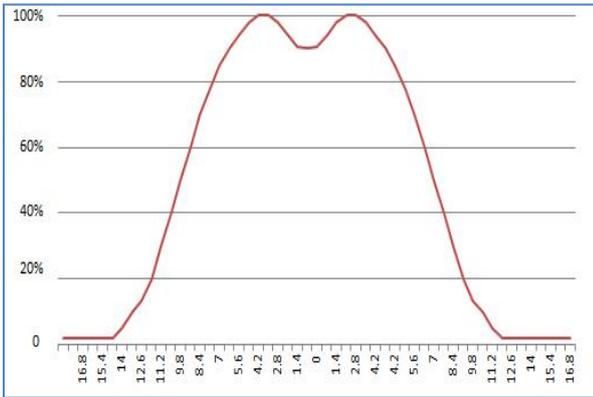
Figure 7.5.1 Typical Laser Diode Beam Divergence
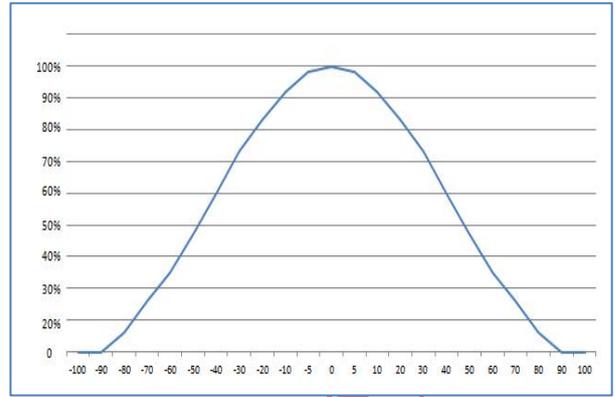
Figure 7.5.2 Typical Photodiode FOV View

@ T = 25℃, VDD = 3.3V, PWT = 400ms, LD Current = 12.5mA, LD on time = 512us.
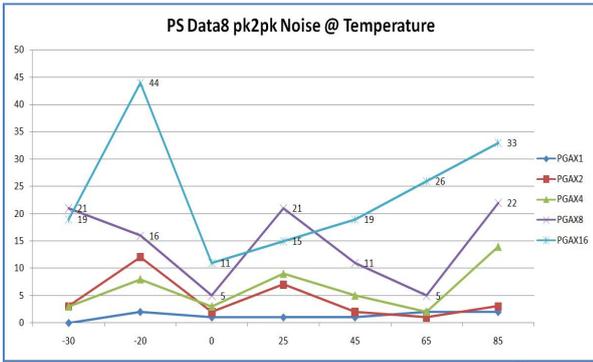

Figure 7.5.3 Typical Peak-to-Peak Noise Code Variation
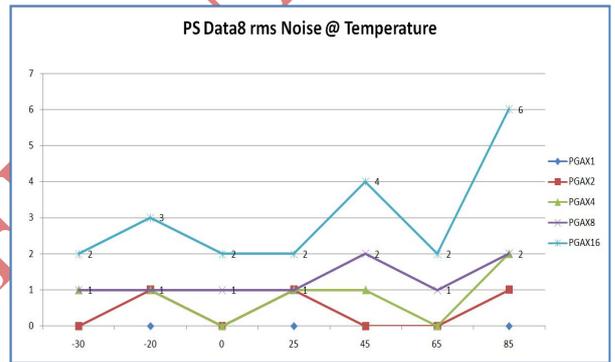
Figure 7.5.4 Typical RMS Noise Code Variation

@ T = 25℃, VDD = 3.3V, PWT = 400ms, LD Current = 12.5mA, LD on time = 512us.
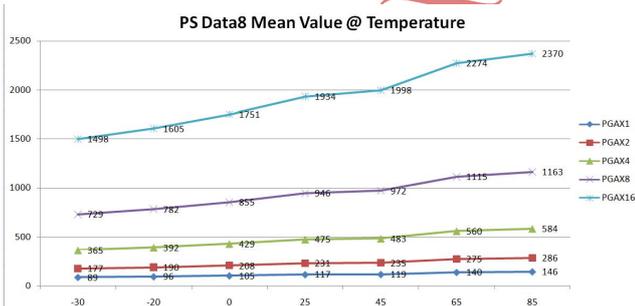
Figure 7.5.5 Typical Mean Value @ Temperature

8 Detailed Description

8.1 Overview

HX3002 is an ultra-low power integrated proximity sensor with a built-in IR Laser Diode (LD) and I2C interface in 2×1.6mm 6pin package (MSL3). It incorporates a Photo-Diode(PD), Programmable Gain Amplifier(PGA), an Offset Current DAC(iDAC) , System Oscillator(OSC32KHz) , Digital Timing Controller(OSC1MHz) and ADC Block in the same chip and also incorporates an Infrared Laser Diode (IR-LD) and built-in Laser Driver with excellent driving performance. The photodiode spectral response is optimized for wavelength 940nm infrared light. HX3002 provides programmable Laser On-Time setting to drive IR-LD and employs noise cancellation scheme to obtain the loop dynamic range of 100dB. For short distance detection use,The powerful on-chip digital engine can automatically eliminate the crosstalk light induced by structural reflection.The maximum structural reflection cancellation range is 100X to the weak useful IR light current. HX3002 also has excellent Auto Ambient Light Suppression Function, and its suppression ratio can as high as 65dB under maximum 100k LUX light intensity. For Single-Master-to-Multi-Slave applications, HX3002 Supports 1-Master-to-2-Slave Mode: Users can dynamically reconfigure one HX3002's I2C address to 0x45 and keep the other one to originally 0x44, thus the master can communicate with the two devices simultaneously through the same I2C Bus line.

8.2 Functional Block Diagram
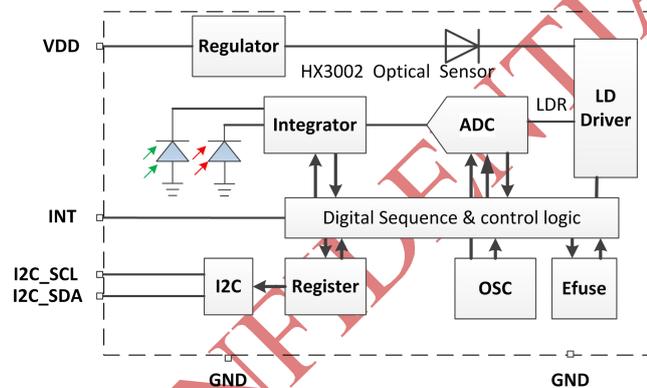
Figure 8.2.1 Functional Block Diagram

8.3 Digital State Machine Diagram

HX3002 has mainly three operation modes:

1 S**leep mode**, which is configured by Power-down (PD) register. All the circuits except I2C are shut down and the power consumption is less than 0.1uA.

2 N**ormal mode (**including **Prox Check** and **Prox ADC),** all the circuits are working to perform proximity sensing.

3 **Standby mode** (PRF Wait), All the circuits except I2C and OSC32KHz clock are shut down to save power.
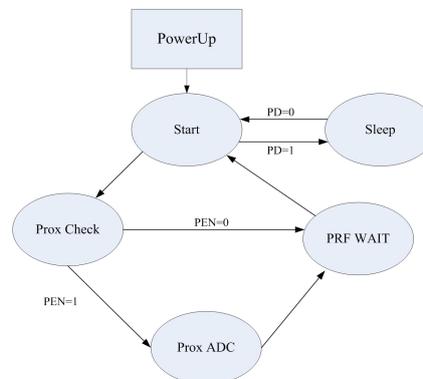
Figure 8.3.1 State Machine Diagram

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8.4 Timing Diagram

The timing information of HX3002 is as following. The device works under two internal clocks: 32KHz system clock DCLK32K and 1MHz ADC timing clock CLK1M. The 32KHz clock is running all the time unless in chip **sleep mode**. It generates the waiting time configured by register **0x01**. The 1MHz high frequency clock only enabled in **normal mode**, and used to provide timing source for ADC and other high clock circuits.
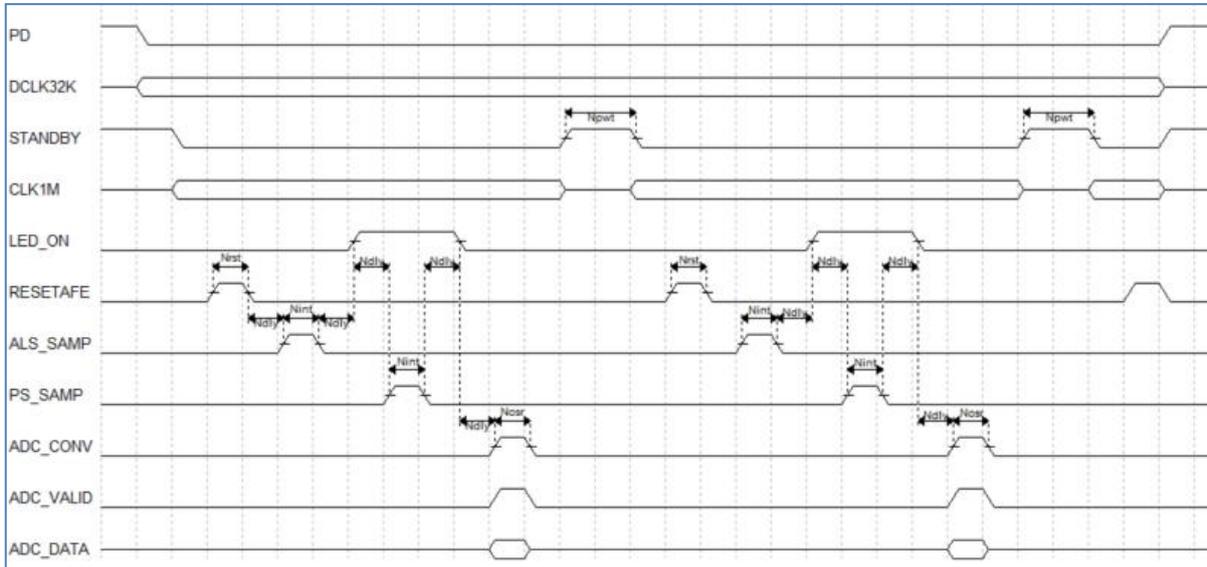
Figure 8.4.1 Main Timing Diagram

8.4.1 ADC Data conversion state Timing Setting(base on 1MHz clock)

RESETAFE   : register 0x02,   selectable in 511, 1023, 2047, 4095 No. of Tclk1mhz, recommend 511* Tclk1mhz;
PS_SAMP   : register 0x03<6:4>, selectable in 64, 128, 256,512, 1024, 2048, 4096 No. of Tclk1mhz, recommend 1024*Tclk1mhz;
ALS_SAMP   : register 0x03<2:0>, selectable in 64, 128, 256,512, 1024, 2048, 4096 No. of Tclk1mhz, recommend 1024*Tclk1mhz;
ADC_CONV   : register 0x01<2:0>, selectable in 1024, 2048, 4096,8192, 16384, 32768, 65535 No. of Tclk1mhz, recommend 4096* Tclk1mhz;

8.5 Offset IDAC

The Built-in Offset Current DAC (iDAC) can cancel the crosstalk light induced by structural imperfection, and the cancellation ratio can be 100x to the useful photodiode current. The Offset iDAC current range is selectable from 12.5nA to 800nA, and is controlled by two registers (**0x21 bit<3:2>** and **0x13 bit<3:0>**).
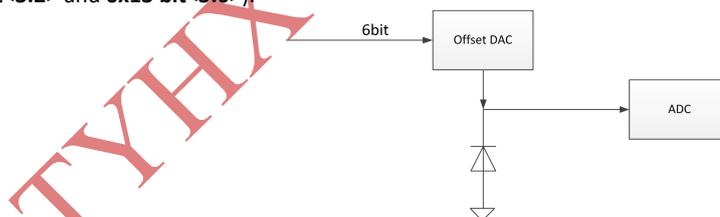
Figure 8.5.1 Offset iDAC

8.6 LD Driver

The device has one internal current DAC with 2bits output range control. The DAC output range is controlled through register **0x13 bits<5:4>**(00=6.25mA, 01=9.375mA, 10=12.5mA, 11=18.75mA)
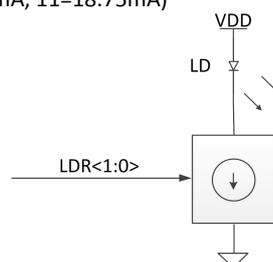
Figure 8.6.1 LD driver circuit

8.7 Analog-to-Digital Converter (ADC)

The receiver path has a high precision sigma-delta ADC that provides a largest 16-bit representation of the current from the photodiode. The ADC has configurable over sampling ratio (OSR) set by register **0x01 bit<2:0>**. The ADC output code corresponding to the photodiode current can be read out from two 16-bit registers (**0x07~0x08**) in unipolar straight binary format.The default ADC full-scale input range is 100nA and the default PGA Gain is 8X. The mapping of the ADC input current to the ADC output code is shown in the table below.

ADC over sample rate = 4095

INPUT CURRENT AT ADC INPUT	12-BIT ADC OUTPUT CODE (Binary)	16-BIT ADC OUTPUT CODE (Decimal)
0	0000_0000_0000_0000	0
800nA	0000_1111_1111_1111	4095

ADC over sample rate = 65535

INPUT CURRENT AT ADC INPUT	16-BIT ADC OUTPUT CODE (Binary)	16-BIT ADC OUTPUT CODE (Decimal)
0	0000_0000_0000_0000	0
800nA	1111_1111_1111_1111	65535

8.8 I2C Address Software Selectable

For Single-Master-to-Multi-Slave application, HX3002 Supports 1-Master-to-2-Slave Mode: No extra pin or resistor needed, through I2C commands, Users can dynamically switch one HX3002's I2C address to 0x45 while keep the other to originally 0x44, thus the master can communicate with the two devices simultaneously through the same I2C Bus line.
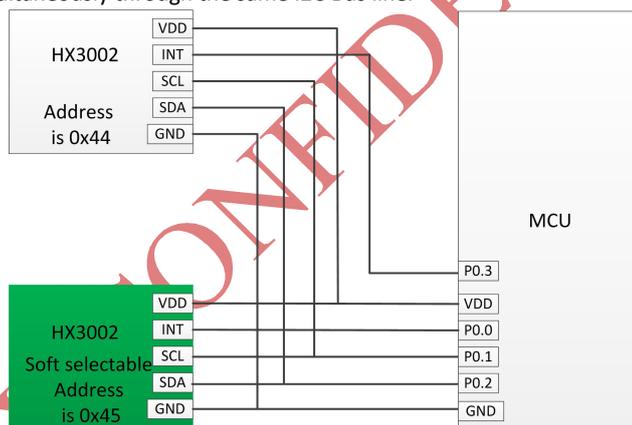
Figure 8.8.1 I2C Address Software Selectable

The default addresses of HX3002 is 0x44, Users can Change the device Address from 0x44 to 0x45 , before the address change operation, make sure the I2C interface SCL and SDA is connected correctly.

Step1: Set the INT pin into OD mode, recommend write reg0x00 with 0x04;
Step2: Read register 0xA5;
Step3: Configure the MCU pin which connected with INT that you want to change address to Output, and out put low voltage;
Step4: Read register 0xA6;
Step5: Release the MCU pin that connected with INT pin to input and this operation can release the INT pin from keeping low;
Step6: Read register 0x45,to make sure that the address change operation work, if not response, repeat step1 to step 5;

8.9 Auto Structural Crosstalk Light Cancellation

HX3002 has built-in auto structure crosstalk light cancellation function. Its work flow is drawn bellow. The powerful on-chip digital engine can automatically eliminate the crosstalk induced by the structural reflection. And maximum cancellation range can be 100X to the weak useful signal current.
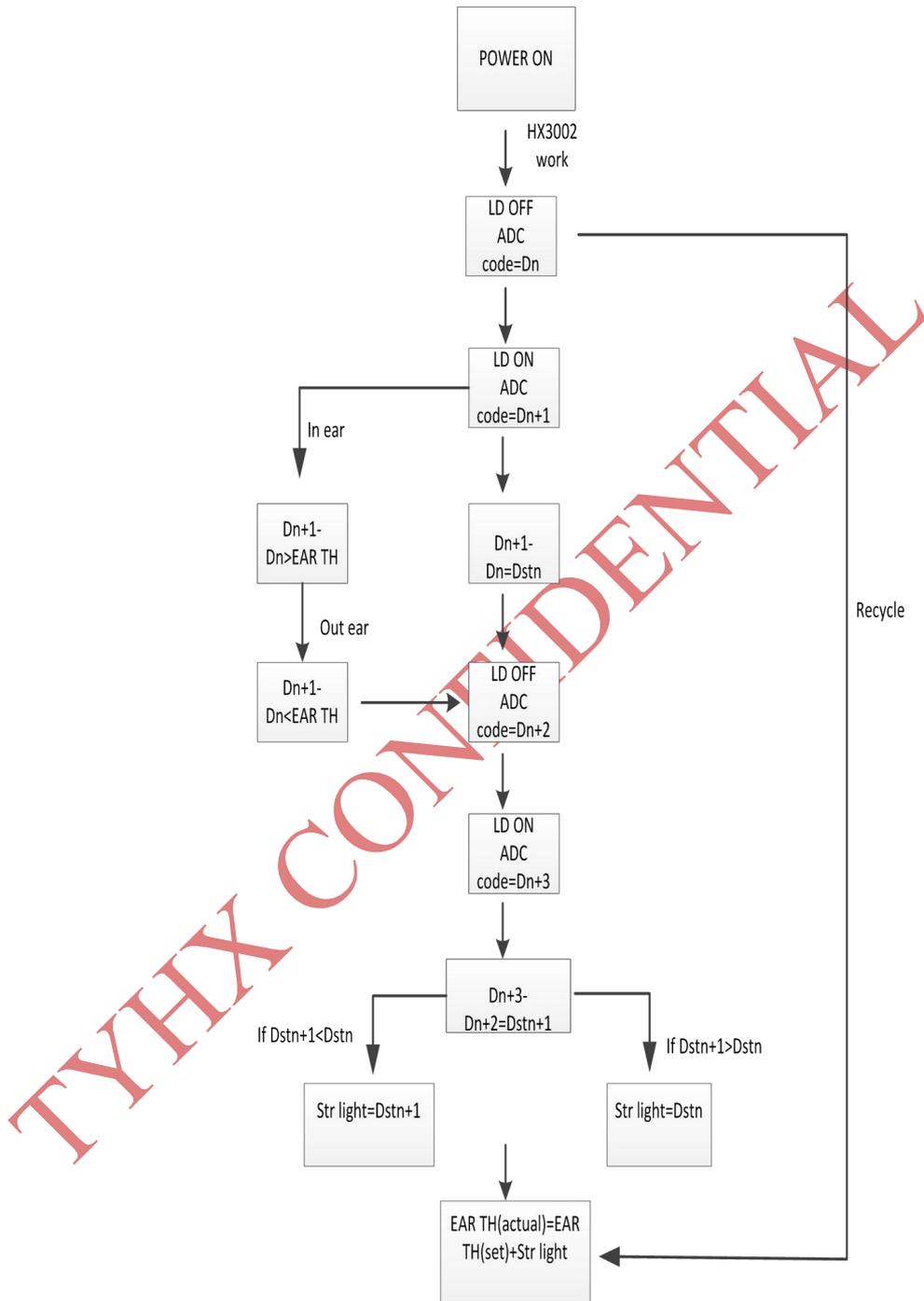
Figure 8.9.1 Structure Crosstalk Light Cancellation Work Flow

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8.10 Intelligent Interrupt Detection

HX3002 includes two Interrupt mode, CMOS Mode and Open Drain (OD) Mode (INT pin output):

1) CMOS Mode Interrupt Output

This is the default interrupt output mode, and is represented simply by voltage level at INT pin (toggle mode):

A: high voltage when ADC code is higher than high threshold value

B: low voltage when ADC code is lower than low threshold value

2) OD Mode Interrupt Output

Open Drain (OD) Mode is set by setting the register 0x00 bit<2>，and the definition of voltage level is the same as CMOS mode:

A: high voltage when ADC code is higher than high threshold value

B: low voltage when ADC code is lower than low threshold value

Both CMOS mode and OD mode, User can also change the interrupt type from toggle mode to I2C clear mode by setting register 0x00 bit<3>. In I2C clear mode, by default, INT pin outputs high voltage. Once triggering interrupt, INT pin outputs low voltage and host processor can clear the interrupt by reading ADC data registers.

3) Intelligent Interrupt Detection

HX3002 incorporates an intelligent detection-interrupt scheme to achieve both fast response and low power. After power-on, by default, HX3002 is in slow response mode (long PS waiting time ~400ms) for low power. Once detecting a change of input signal and the ADC code is lower than low threshold (out-ear state) or higher than high threshold (in-ear state), HX3002 adjusts PS waiting time to about 25ms to speed up the checking of input signal. After accumulating a preset count (for example 1, 4, 8 or 15) of consistent under or over threshold condition, HX3002 triggers the interrupt to report to host processor. If the triggering condition is not met, HX3002 resumes the long waiting time (default 400ms) and goes back to low power mode. This scheme can significantly reduce the false interrupt while still maintaining very low power consumption.

4) INT Trigger Condition Illustration

Count number to trigger the interrupt is set to 4.
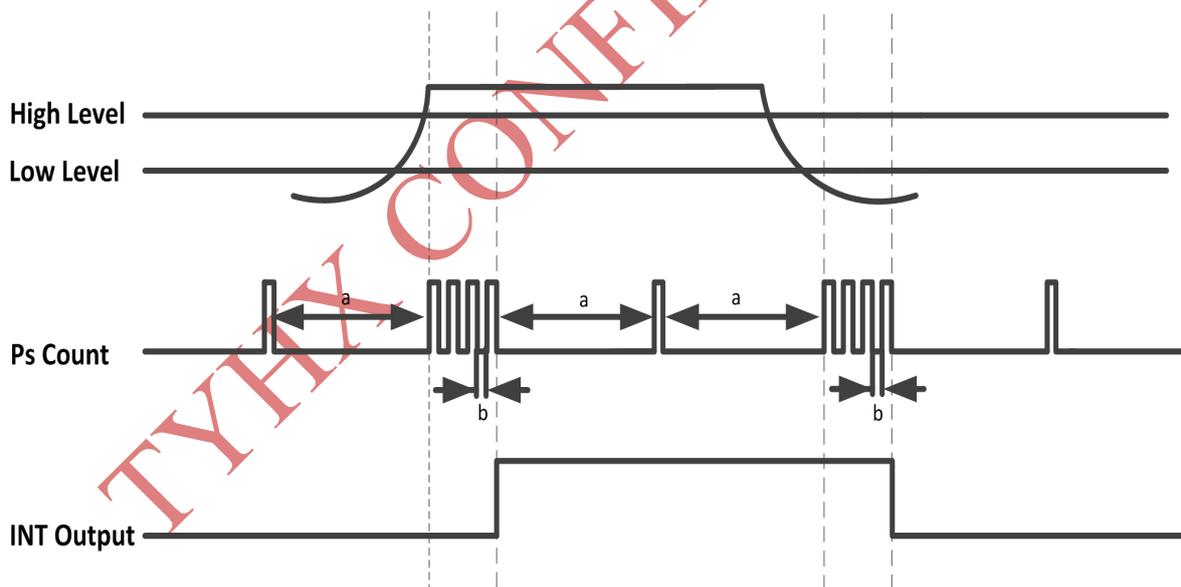
Note :

a : PWT = 400ms

b : PWT= 25ms

Figure 8.10.1   Intelligent Interrupt Scheme

9 Register Map

ADDR=0x00:

Address	Type	Default	Name	BIT	Default	Description
0x00	RW	0x0A	Force_standby_cfg	7	0	1:Standby 0:Not Standby
			Force_standby_sel	6	0	Enable standby 1:Enable 0:Disable
			Reserve	5	0	Reserve
			Reserve	4	0	Reserve
			Int_gen_mode_i2c	3	1	1:Voltage toggle 0:Normal(i2c clear)
			Int mode	2	0	1:OD INT 0:CMOS INT
			PEN	1	1	Enable PEN
			PD	0	0	Enable POWER DOWN

ADDR=0x01:

Address	Type	Default	Name	BIT	Default	Description
0x01	RW	0x5A	Wait_num_i2c	7:4	0101	Waitting time 0000 0ms 0001 25ms 0010 50ms 0011 100ms 0100 200ms 0101 400ms 0110 800ms 0111 1600ms
			Efuse_i2c	3	1	Threshold is seted by efuse 1:Yes 0:No
			Osr_num_i2c	2:0	010	000 :osr_num = 1024 001 :osr_num = 2048 010 :osr_num = 4096 011 :osr_num = 8192 100 :osr_num = 16384 101 :osr_num = 32768 110 :osr_num = 65535

ADDR=0x02:

Address	Type	Default	Name	BIT	Default	Description
0x02	RW	0x50	Int_bigger_num_i2c	7:6	01	Higher than threshold times 00 : int_bigger_num = 1 01 : int_bigger_num = 4 10 : int_bigger_num = 8 11 : int_bigger_num = 15
			Int_lower_num_i2c	5:4	01	lower than threshold times 00 : int_lower_num = 1 01 : int_lower_num = 4 10 : int_lower_num = 8 11 : int_lower_num = 15
			Reserve	3:2		Reserve
			Reserve	1:0		Reserve

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ADDR=0x03:

Address	Type	Default	Name	BIT	Default	Description
0x03	RW	0x4D	Efuse_clk_en	7	0	ENABLE efuse clock 1:Enable 0:Disable
			Ps_samp_num_i2c	6:4	100	Width of PS_SAMP (us) 000:PS_samp_num =0 001:PS_samp_num =64 010:PS_samp_num =128 011:PS_samp_num =256 100:PS_samp_num =512 101:PS_samp_num =1024 110:PS_samp_num =2048 111:PS_samp_num =4095
			Ld on_en	3	1	1:Enable LD 0:Disable LD
			Als_samp_num_i2c	2:0	101	Width of ALS_SAMP (us) 000:ALS_samp_num =0 001:ALS_samp_num = 64 010:ALS_samp_num =128 011:ALS_samp_num =256 100:ALS_samp_num =512 101:ALS_samp_num =1024 110:ALS_samp_num =2048 111:ALS_samp_num =4095

ADDR=0x04-0x06:

Address	Type	Default	Name	BIT	Default	Description
0x04	RW	0x60	Th_high_i2c[7:0]	7:0	01100000	High threshold[1] B11:B4
0x05	RW	0x98	Th_high_i2c[11:8]	7:4	1001	High threshold B15:B12
			Th_low_i2c[11:8]	3:0	1000	Low threshold[2] B15:B12
0x06	RW	0x98	Th_low_i2c[7:0]	7:0	10011000	Low threshold B11:B4

1:Register settings need to be based on High threshold, but High threshold not equal to actual value, here is a simple conversion, High threshold = actual threshold right shift 4 bits , (e.g: the actual threshold is 800, the High threshold is 800>>4 = 50)
Register settings need to be based on Low threshold, but Low threshold not equal to actual value, here is a simple conversion,
Low threshold = actual threshold right shift 4 bits , (e.g: the actual threshold is 600, the Low threshold is 600>>4 = 37)

ADDR=0x07-0x08:

Address	Type	Default	Name	BIT	Default	Description
0x08	RO		RA_ADC_DATA_H	7:0		ADC output high 8bit
0x07	RO		RA_ADC_DATA_L	7:0		ADC output low 8bit

ADDR=0x10

Address	Type	Default	Name	BIT	Default	Description
0x10	RW	0x20	Reserve	7		
			Reserve	6		
			LD current bias	5:0	10000	LD current bias 00000:320uA ..... 10000:640uA 11111:950uA 10uA/step

ADDR=0x11

Address	Type	Default	Name	BIT	Default	Description
0x11	RW	0x77	ADC_DACN	7:4	0111	ADC Signal Process Range 0000 100nA 0001 200nA 0010 300nA 0011 400nA 0100 500nA 0101 600nA 0110 700nA 0111 800nA 1000 900nA 1001 1000nA 1010 1100nA 1011 1200nA 1100 1300nA 1101 1400nA 1110 1500nA 1111 1600nA
			OSCBIAS	3:0	0111	OSCBIAS 0000： 58% 0111： 100% 1111： 147% 5.875%/step

ADDR=0x12

Address	Type	Default	Name	BIT	Default	Description
0x12	RW	0x74	PD PGA	7:4	0111	Photo diode Light Current Gain Select 0000 1X 0001 2X 0010 3X 0011 4X 0100 5X 0101 6X 0110 7X 0111 8X 1000 9X 1001 10X 1010 11X 1011 12X 1100 13X 1101 14X 1110 15X 1111 16X 1X/step
			THOD	3:0	0100	High threshold

Remark :Threshold

3:0	THODH/dec	THODL/dec
L0	704	496
L1	912	704
L2	1120	912
L3	1328	1120

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L4	1536	1328
L5	1744	1536
L6	1952	1744
L7	2160	1952
L8	2368	2160
L9	2576	2368
LA	2784	2576
LB	2992	2784
LC	3200	2992
LD	3408	3200
LE	3616	3408
LF	3824	3616

ADDR=0x13:

Address	Type	Default	Name	BIT	Default	Description
0x13	RW	0x60	Reserve	7	0	Reserve
			Structure light cancel enable	6	1	1:Enable 0:Disable
			LD drive current	5:4	10	00 :6.25mA 01:9.375mA 10:12.5mA 11:18.75mA
			Reserve	3:0	0000	Reserve

ADDR=0x20

Address	Type	Default	Name	BIT	Default	Description
0x20	RW	0x88	ADC_IBSEL<3:0>	7:4	1000	ADC current bias trimming 0000　　100nA 0001　　112.5nA 0010　　125nA 0011　　137.5nA 0100　　150nA 0101　　162.5nA 0110　　175nA 0111　　187.5nA 1000　　200nA 1001　　212.5nA 1010　　225nA 1011　　237.5nA 1100　　250nA 1101　　262.5nA 1110　　275nA 1111　　287.5nA
			AFE_RCTRIM<3:0>	3:0	1000	Reserve

ADDR=0x21

Address	Type	Default	Name	BIT	Default	Description
0x21	RW	0xD3	IRPDSEL<1>	7	1	ALS /IR PD Enable 0:Enable PS PD 1:Enable (ALS PD + PS PD)
			IRPDSEL<0>	6	1	ALS Sample Reset 0:Disable ALS phase 1:Normal work with ALS phase
			I1P8SEL	5	0	1.8V IO Terrence Select 0:1.8V 1:3.3V
			CKDIVSEL	4	1	OSC_2M_core ouput choose, 0 :div1 1: div2 output 1MHz
			Reserve	3:2	00	Reserve
			OSCTEST<1:0>	1:0	11	OSC Test; 11------ INT Output 10------ MCLK1M 01------ DCLK32K 00------ PDON_RST （Reserve）

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10 Digital Interface

10.1 I2C

10.1.1 I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device addresses 0x44. The register index will automatically increaseby1after the addresses register has been accessed(read or write).And the format is shown as following:

A   Acknowledge (0)

P   Stop Condition

R   Read (1)

S   Start Condition

W   Write (0)

Sr   Repeated Start Condition

■   Master-to-Slave
□   Slave-to-Master

I2C Write Register Data
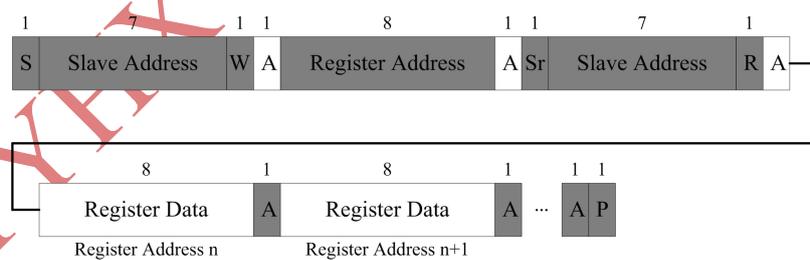
I2C Read Register Data

Figure 10.1.1 I2C Data Format Diagram

10.1.2 I2C AC Timing

Table10.1.1Characteristics of the SDA and SCL I/O stages for F/S-mode I2C-bus devices

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
LOW level input voltage: fixed input levels VDD-related input levels	VIL	-0.5 -0.5	1.5 0.3VDD	n/a -0.5	n/a 0.3VDD (1)	V V
High level input voltage: fixed input levels VDD-related input levels	VIH	3.0 0.7VDD	(2) (2)	n/a 0.7VDD (1)	n/a (2)	V V
Hysteresis of Schmitt trigger inputs: VDD > 2 V VDD < 2 V	Vhys	n/a n/a	n/a n/a	0.05VDD 0.1VDD	–	V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2 V VDD < 2 V	VOL1 VOL3	0 n/a	0.4 n/a	0 0	0.4 0.2VDD	V V
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 Pf	Tof	–	250(4)	20 + 0.1Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	TSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	1-10(5)	10(5)	mA
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1. Devices that use non-standard supply voltage switch don't conform to the intended I^2C-bus system levels must relate input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.

2. Maximum V_{IH} = V_{DDmax} + 0.5V.

3. C_b = capacitance of one bus line in pF.

4. The maximum t_f for the SDA and SCL bus lines quoted in Table2(300ns) is longer than the specified maximum t_{of}

5. for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL

6. pins and the SDA/SCL bus lines as shown in Fig.10.1.1without exceeding the maximum specified t_f.

7. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

   n/a = not applicable

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Table10.1.2 Characteristics of the SDA and SCL bus lines for F/S-mode I2C-bus devices(8)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	FSCL	0	100	0	400	kHz
Hold time (repeated) START condition.After this period, the first clock pulse is generated	THD;STA	4	–	0.6		us
LOW period of the SCL clock	TLOW	4.7	–	1.3	–	us
HIGH period of the SCL clock	THIGH	4	–	0.6	–	us
Set-up time for a repeated START condition	TSU;STA	4.7	–	0.6	–	us
Data hold time	THD;DAT	0(9)	3.45(10)	0(2)	0.9(10)	us
Data set-up time	TSU;DAT	250		100(11)	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20 + 0.1Cb(12)	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20 + 0.1Cb(12)	300	ns
Set-up time for STOP condition	TSU;STO	4	–	0.6	–	us
Bus free time between a STOP and START condition	TBUF	4.7	–	1.3	–	us
Capacitive load for each bus line	Cb	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	VnL	0.1VDD	–	0.1VDD	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	VnH	0.2VDD	–	0.2VDD	–	V

Notes

8. All values referred to V_{IHmin} and V_{ILmax} levels (see Table1).

9. A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

10. The maximum $T_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (T_{LOW}) of the SCL signal.

11. A Fast-mode I2C-bus device can b eusedinaStandard-modeI2C-bussystem,but the require meant TSU;DAT 250ns must the be met.This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such advice does stretch the LOW period of the SCL signal,it must output the next data bit to the SDA line t_{rmax}

12. + TSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. C_b=total capacitance of one bus line in pF.If mixed with HS-mode devices,faster fall-times according to Table6 are allowed.

n/a = not applicable
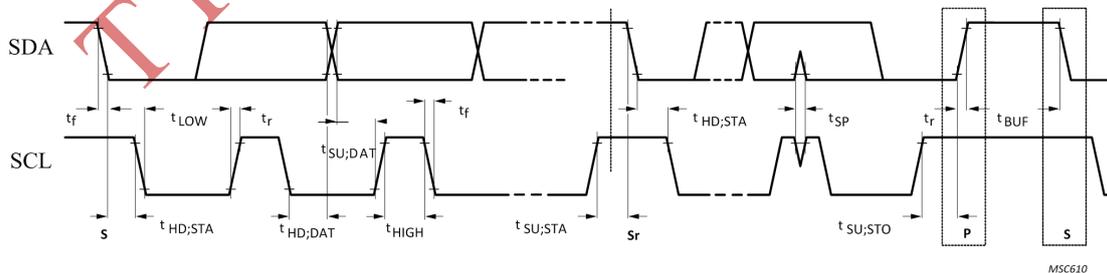
Figure 10.1.2 I2C Timing Diagram

11 Application Information

Typical application for HX3002 is showing below:

### 11.1 VDD = IIC VBUS , CMOS mode INT
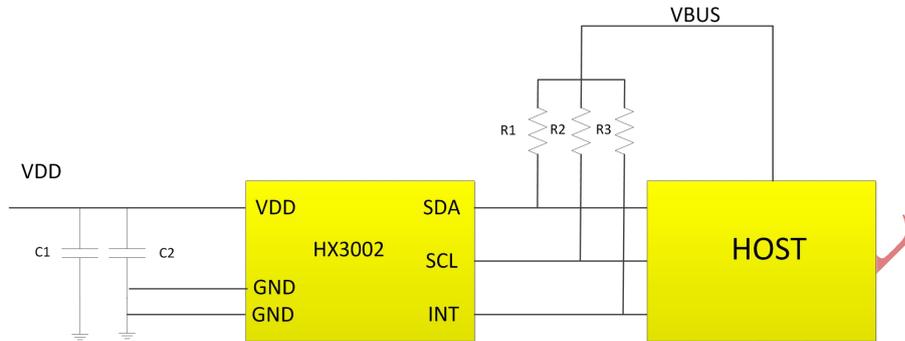
Figure 11.1 Typical Application Schematic

And the device value is listed below:

DEVICE NAME	Value	Description
VDD	2.9~3.6 V	Low noise
VBUS	VDD	
C1	4.7uF	
C2	0.1uf	
R1	10 KΩ	
R2	10 KΩ	
R3	NC	

11.2 IIC VBUS=1.7-2V , OD mode INT
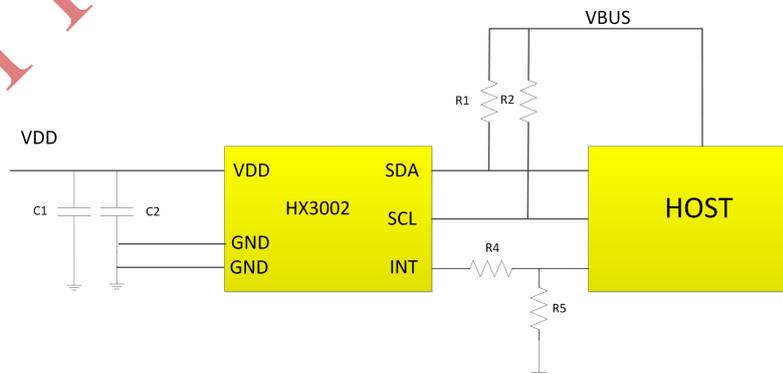
DEVICE NAME	Value	Description
VDD	2.9~3.6 V	Low noise
VBUS	VDD	
C1	4.7uF	
C2	0.1uf	
R1	10 KΩ	
R2	10 KΩ	
R4	Decided by VBUS[1]	More than 100K
R5	Decided by VBUS[1]	More than 100K

1:VDD*R5/(R4+R5)= VUS

12 Package Information

Unit: mm   Tolerance: ±0.1
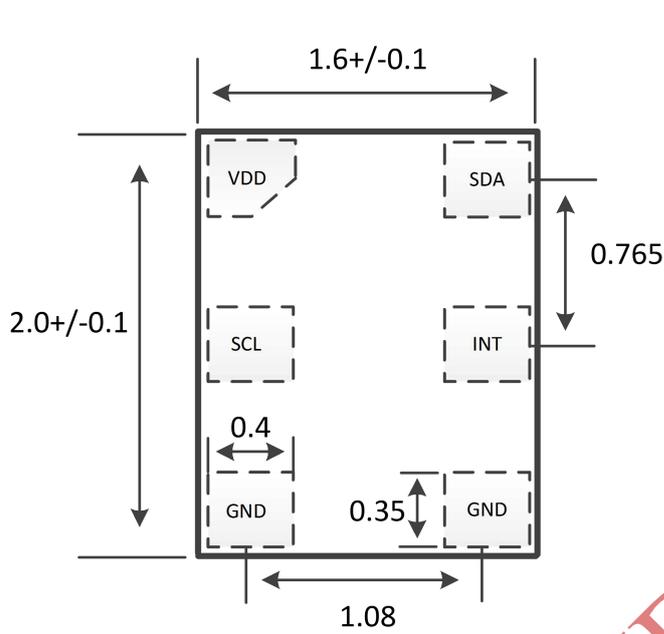
Figure 12.1 Package Top View

Figure12.2 Package Side View
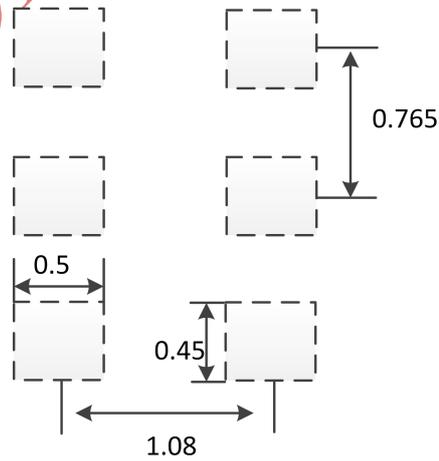
Figure 12.3 Land Pattern View

13 Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate ,the process,equipment material use din these test are detailed below, the solder reflow profile describes the expect maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.
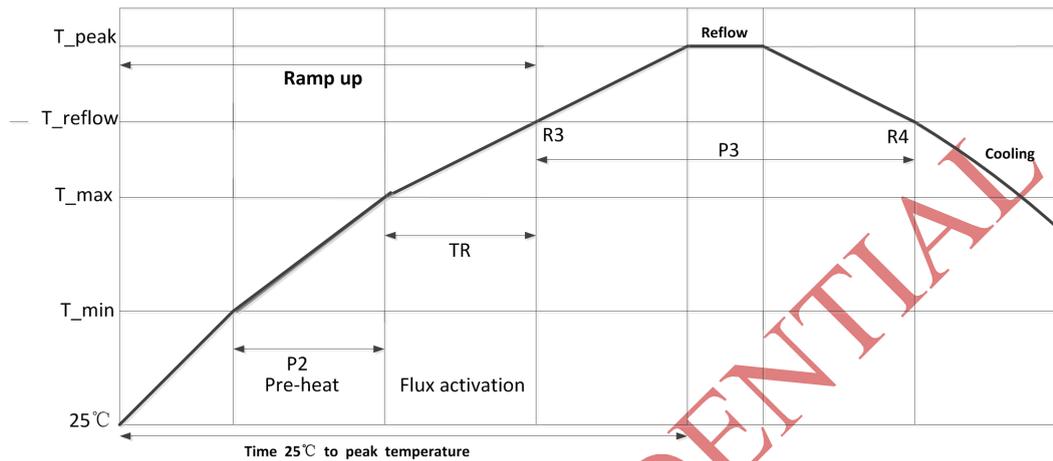

Figure 13.1 Solder Reflow Profilegrape

Table13.1 Solder Reflow Profile

	Peak temperature (Tpeak)	240-250℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃；100S to 180S
	P2：（T min to max）	90-110s
Time maintain above	Temperature (Treflow)	217 ℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

14 Packing Information
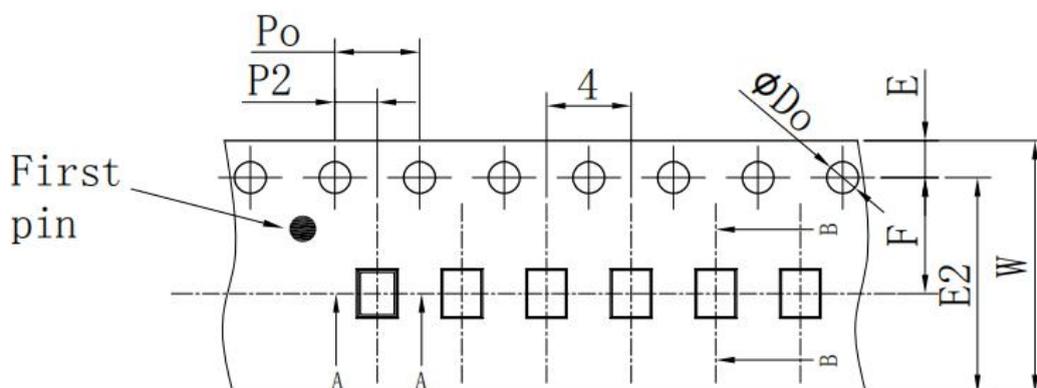
SIZE	
E	1.75±0.10
E2	10.25 MIN
F	5.50±0.10
P2	2.00±0.10
ΦDo	1.50±$^{0.10}_{0.00}$
ΦD1	
Po	4.00±0.10
10Po	40.00±0.20
W	12.00±0.30
P	4.00±0.10
Ao	1.80±0.10
B0	2.20±0.10
K0	0.90±0.10
t	0.30±0.05

0.9   1.8

A-A

2.2

0.3

B-B
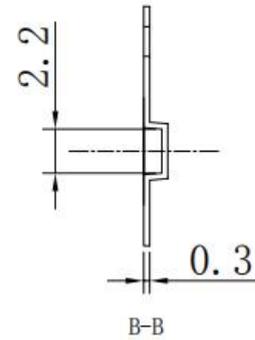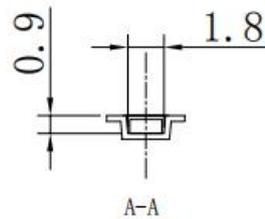
Change List			
V1.0	Initial	Tom Zhao	2019.10.20
V1.1	Added register description	Tom Zhao	2021.01.08
V1.2	Added register description	Tom Zhao	2021.01.12
V1.3	Added register description	Tom Zhao	2021.01.20
V1.4	Added register description	Tom Zhao	2021.01.26
V1.5	Added register description	Tom Zhao	2021.02.28
V1.6	Added circuit description	Tom Zhao	2021.07.20