HX3690S Data Sheet v1.0

Product Definition

HX3690S is an ultra-low power Integrated AFE for Optical, Heart-Rate Monitor and Bio-sensor,and a capacitance sense AFE is integrated for the wearable detection.

Description

HX3690S is an ultra-low power integrated AFE for Wearable, Optical, Heart-Rate Monitor and Bio-sensor with I2C interface. HX3690S include PPG and SAR(Specific Absorption Rate) two parts. The PPG part have two input channels, ±64uA offset IDAC,three fully-integrated LED drivers with 8-bit current control and and a high resolution ADC .The SAR part has high sensitivity which enables the detection of human body proximity and supports up to two sensor inputs, with an offset compensation capacitance up to 50pF.The device has a high dynamic range transmit and receive circuitry that helps with the sensing of very small signal.

Features

PPG:

Accurate, Continuous Heart-Rate Monitoring:

1. Better than 100-dB dynamic range for accurate heart-rate detection
2. Support four phase data in each conversion period
3. Low power for continuous operation on a wearable device with a typical value:
   20 μA for an LED, 45 μA for the Receiver

@ FS=25Hz， LED on time = 32uS , LED driver = 25mA

Transmitter:

1. 8-Bit programmable LED current to 200 mA
2. Programmable LED on time from 8us to 1024us
3. Support 3 LEDs for optimized SpO2, HRM, and off-wrist detection
4. Ultra-low current of 20μA is adequate for a typical heart-rate monitoring scenario:

@ FS=25Hz, LED on time = 32uS, LED driver = 25mA

Receiver:

1. 21-Bit representation of the current Input from a photodiode in unipolar straight binary format
2. Individual DC offset subtraction IDAC (Up to ±64μA) at TIA input for each phase
3. Integrator gain adjustment tia. range 10K to 1M.
4. Software sleep mode: approximately 1.5 μA current

SAR:

1. Two sensor inputs
2. Capacitance resolution up to 1aF
3. Capacitance offset compensation up to 50pF
4. Support fully differential input mode
5. Smart SAR detection engine
6. Programmable scan period from 10ms to 200ms
   Programmable detection range
   Programmable Interrupt or Real-Time Status Pin

Pulse Frequency: 1 SPS to 1000 SPS
FIFO With 64-Sample Depth
I2C Interface
Operating Temperature Range: -20℃ to 85℃
Supplies:

1. TX_SUP =3.0 V~5.25 V
2. VDDA =2.7 V~3.6 V
3. IO_SUP = 1.8 V~VDDA
4. VDD=1.65 V~1.8 V

Applications

1. **Optical Heart-Rate Monitoring (HRM)**
2. **Heart-Rate Variability (HRV)**
3. **Pulse Oximetry (SpO2) Measurements**
4. **Maximum Oxygen Consumption (VO2 Max)**

PKG Information

3.0×3.0×0.75mm QFN20

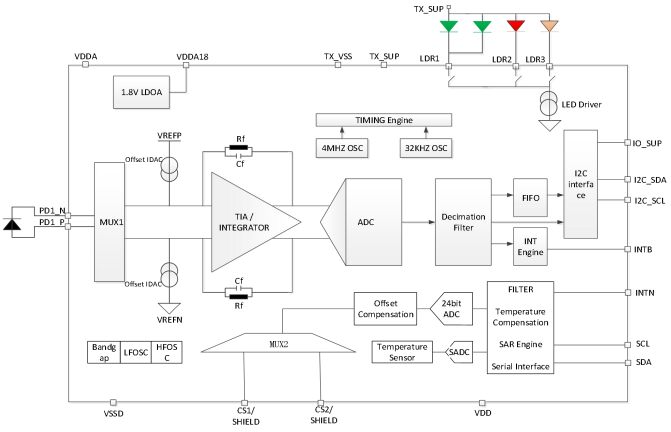

Figure 1.Simplified Block Diagram

CONTENTS

Pin Configuration

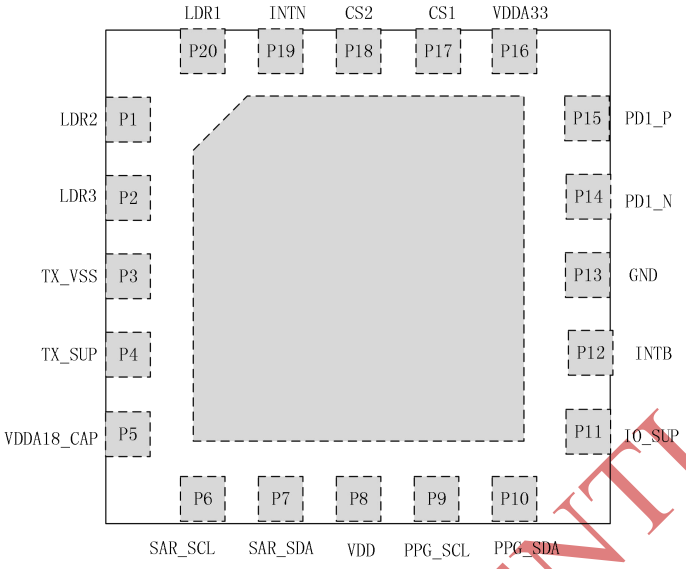

Figure 2. HX3690S Top View Pin Configuration

PIN List

Table 1 HX3690S PIN list

Pin	Name	Type	Description
1	LDR2	A	LED driver2, up to 200Ma
2	LDR3	A	LED driver3, up to 200Ma
3	TX_VSS	A	Power supply ground for LED drivers
4	TX_SUP	A	Power supply for LED drivers
5	VDDA18_CAP	A	Internal 1.8V LDO output, need 10uf capacitor to GND
6	SAR_SCL	D	SAR I2C CLK, external pull up resistor
7	SAR_SDA	D	SAR I2C SDA, external pull up resistor
8	VDD	A	SAR power supply
9	PPG_SCL	D	PPG I2C SCL, external pull up resistor
10	PPG_SDA	D	PPG I2C SDA, external pull up resistor
11	IO_SUP	A	PPG digital IO power supply
12	INTB	D	CMOS output, PPG ADC conversion ready interrupt signal and FIFO INT signal
13	GND	A	Power ground
14	PD1_N	A	External photo diode cathode input pin
15	PD1_P	A	External photo diode anode input pin
16	VDDA	A	PPG receiver power supply
17	CS1	A	Capacitance Sensor Input1
18	CS2	A	Capacitance Sensor Input2
19	INTN	D	SAR ADC conversion ready interrupt signal
20	LDR1	A	PPG LED driver01, up to 200Ma

Specifications

Absolute Maximum Rating(T_a=25℃, unless otherwise specified)

Parameter	Min	Max	Unit
PPG			
VDDA to VSS	-0.3	4	V
Input Voltage	VDDA – 0.3	VDDA + 0.3	V
Input current	-7	7	mA
SAR			
VDD to VSS	-0.5	2	V
Input Voltage	-0.5	VDD+0.3	V
Input current	-10	10	mA
UNIVERSAL			
Operating temperature range	-20	85	℃
Maximum junction temperature		125	℃

Recommended Operating Conditions

Parameter	Min	Max	Unit
VDDA	2.7	3.6	V
TX_SUP	3.0	5.25	V
IO_SUP	1.8	VDDA	V
VDD	1.65	1.98	V
Supply voltage accuracy	±2		%
Specified temperature range	-20	85	℃
Maximum junction temperature		125	

ESD Ratings

		Value	Unit
V(esd) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±250	

Electrical Characteristics

Minimum and maximum specifications are at TA = –20°C to 85°C, typical specifications are at 25°C. VDD=1.8V,VDDA=3.3V, TX_SUP= 4V, 25Hz date output rate, LED driver current 25mA, led on time= 32uS, 32KHz and 4MHz internal clock, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PPG					
PULSE REPETITION FREQUENCY		1		1000	SPS
RECEIVER					
Offset cancellation DAC current range	7-bit IDAC	-64		64	uA
Offset cancellation DAC current step			500		nA
TIA gain setting (Rf)	3 bit control	10K		1M	Ω
TRANSMITTER					
LED current range	6 bit control	0		200	mA
LED on time	8 bit control	0		1024	uS
CLK (Internal 4MHz Oscillator , used to generate ADC timing)					
Frequency			4		MHz
Accuracy	Room temperature		±1%		
Frequency drift with temperature	Full temperature range		±0.5%		
CLK (Internal 32KHz Oscillator , used to generate PRF and INT timing)					
Frequency			32		KHz
Accuracy	Room temperature		±1%		
Frequency drift with temperature	Full temperature range		±0.5%		
I2C INTERFACE					

Maximum clock speed		800			KHz
I2C slave address		0x44(7bit)			HEX
PERFORMANCE					
Receiver DR(dynamic range)		104			dB
Transmitter DR(dynamic range)		92			dB
CURRENT CONSUMPTION					
Receiver current	Data conversion state	< 550			uA
	PRF wait state	< 40			uA
	Solftware sleep state	< 2			uA
TX LED current	Normal operation	20(2)			uA
	Solftware turnoff mode	< 0.1			uA
SAR					
Conversion Rate		10		200	ms
Resolution		4		100	aF/LSB
Input Range		0.625		5	pF
Input Channel Linearity			±3		fF
Sampling Frequency		4		800	kHz
RMS Noise @30pF load			30		aF
RMS Noise @200pF load			200		aF
Input Leakage				1	nA
Gain Error				3	%
Offset Compensation Range				50	pF
Offset Compensation Resolution			50		fF
Input RC Resistor		400		4k	Ω
Input RC Capacitor			5		pF
Total Internal Channel Capacitance			6		pF
Current Consumption					
Full Power	1KHz conversation rate		1.1		mA
Scan Mode	Single channel, ODR=5Hz		25		μA
Doze Mode	ODR=2.5Hz		7		μA
Sleep Mode			1.6		uA
INTERNAL OSCILLATOR					
HFOSC Frequency			5		MHz
HFOSC Accuracy				±4	%
LFOSC Frequency			32		kHz
LFOSC Accuracy				±4	%
POWER-ON RESET					
Power-Down Level				0.2	V
Power-On Level		1.5			V
VDD		1.65		1.98	V
UNIVERSAL					
DIGITAL INPUTS					
High-level input voltage		0.9*IO_SUP		IO_SUP	V
Low-level input voltage		0		0.1*IO_SUP	V
DIGITAL OUTPUTS					
High-level output voltage		IO_SUP			V
Low-level output voltage		0			V

(1) PRF refers to the rate at which samples from each of the four phases are output from the AFE.

(2) I_tx = 25mA*32uS/40mS = 20uA

Typical Characteristics

@ T = 25℃, TX_SUP=4.0V, VDDA = 3.3V, VDD =1.8V,PRF = 25Hz, ODR = 5Hz, LED on time = 32uS , Rf = 150K,Cf is adjusted to keep the TIA time constant at 1/10th of the sample time(same to led on time) ,SNR (dBFS) = noise referred to full-scale range of 1.8V, noise integrated from 1 Hz to Nyquist (= PRF / 2) .

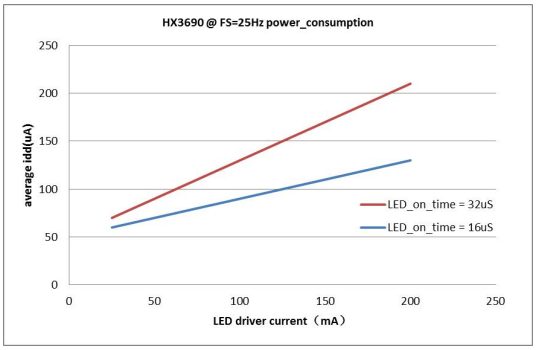

Figure 3. Typical HRM power consumption vs LED driver current

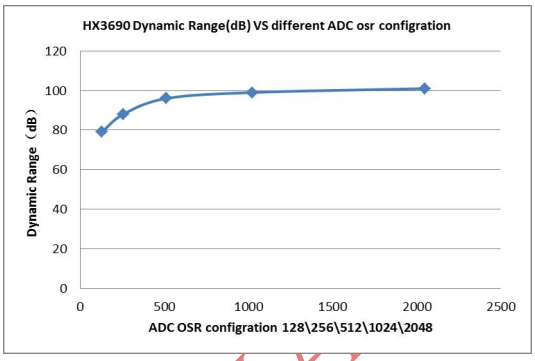

Figure 4. Dynamic Range vs Different OSR

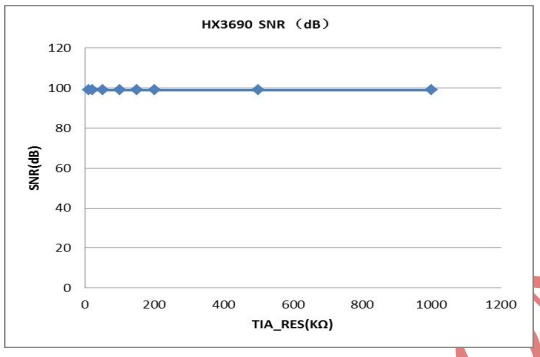

Figure 5. Receiver SNR vs Different TIA Gain Settings

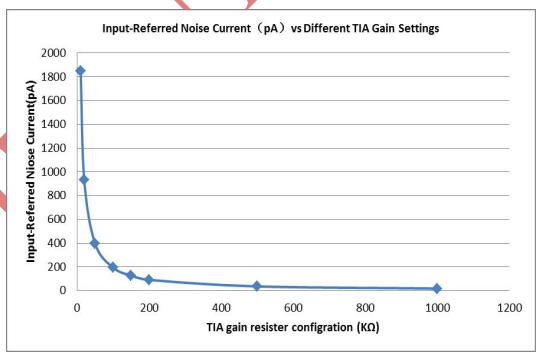

Figure 6. Receiver Input-Referred Noise Current vs Different TIA Gain Settings

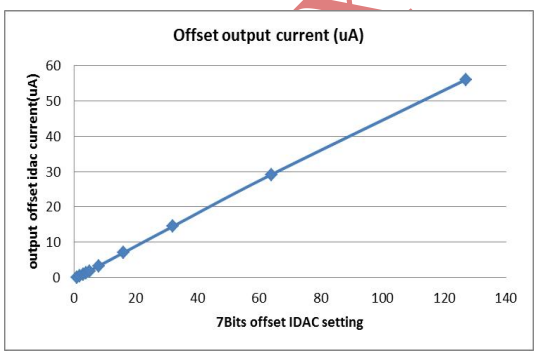

Figure 7. 7bits control offset IDAC output current

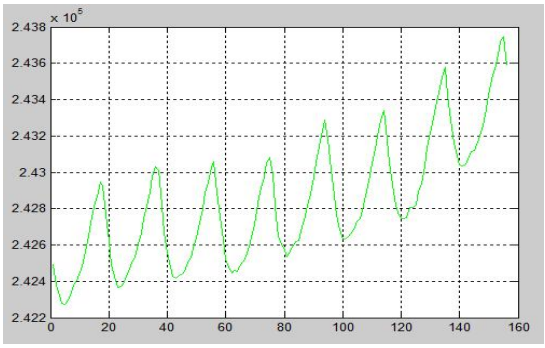

Figure 8. Wrist PPG waveform under typical HRM setting@ average 65uA

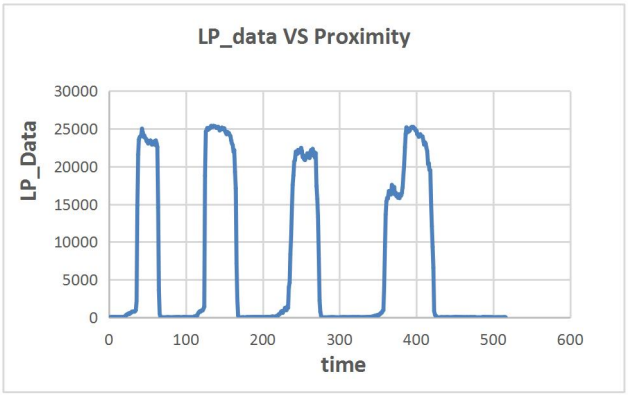

Figure 9. Typical LP data vs Proximity

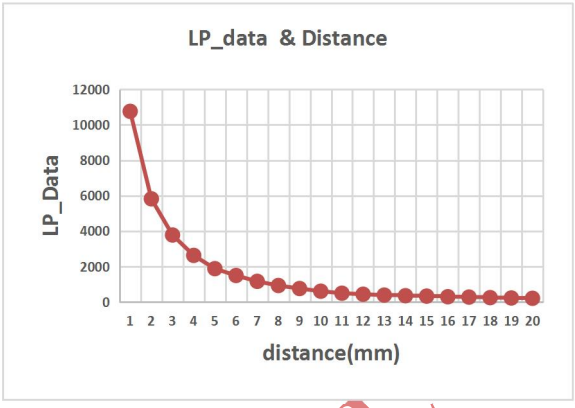

Figure 10. Typical LP data vs Distance

Typical Characteristics(continued)

@ T = 25℃, TX_SUP=4.0V, VDDA = 3.3V, PRF = 25Hz, LED on time = 32uS , Rf = 150K,Cf is adjusted to keep the TIA time constant at 1/10th of the sample time(same to led on time) ,SNR (dBFS) = noise referred to full-scale range of 1.8V, noise integrated from 1 Hz to Nyquist (= PRF / 2) .

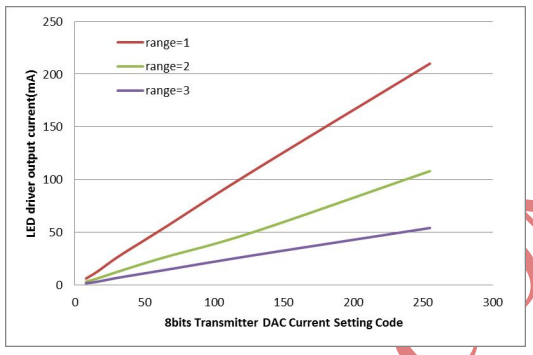

Figure 11. Transmitter Current Linearity

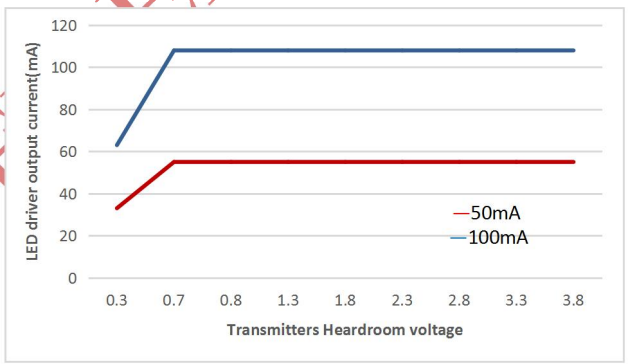

Figure 12. LED Current vs Transmitter Headroom Voltage

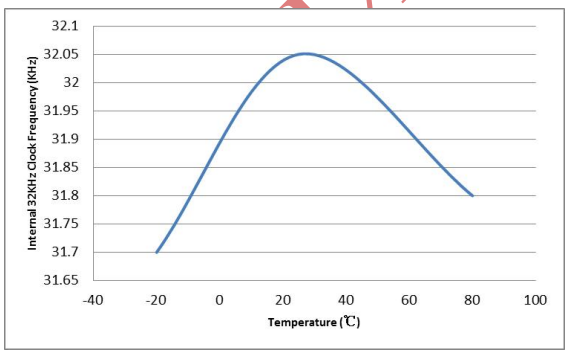

Figure 13. 32KHz Internal Oscillator Frequency vs Temperature on a Typical Unit

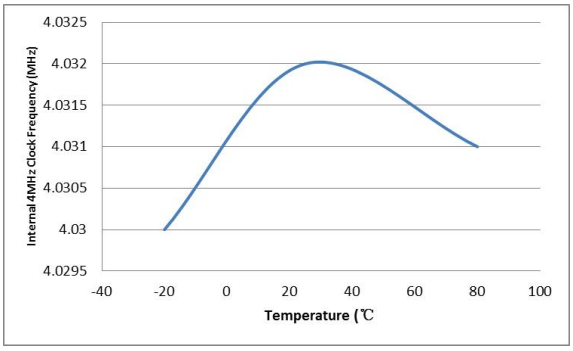

Figure 14. 4MHz Internal Oscillator Frequency vs Temperature on a Typical Unit

Detailed Description

Overview

HX3690S internally integrates transmitter and receiver for optical heart rate monitoring and pulse oxygen saturation measurement applications. The system is characterized by a parameter called pulse repetition frequency (PRF), which determines the repetition period of the operation sequence. Each cycle of PRF generates four 21 bit digital samples at the output of AFE, and each sample is stored in a separate register.

Functional Block Diagram

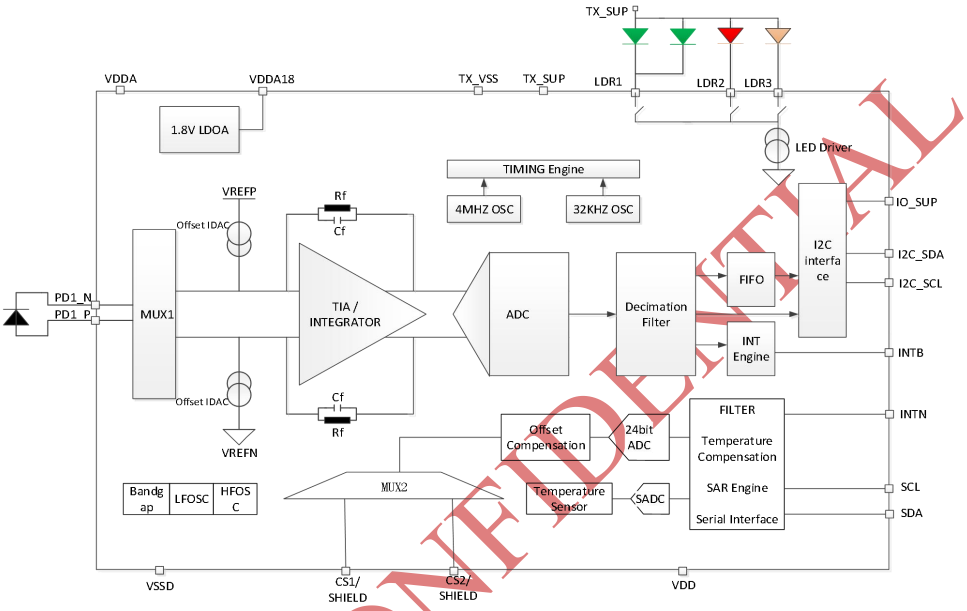

Figure 15. Functional Block Diagram

Digital State Machine Diagram

PPG:

State machine is a synchronous interface for interactive data between digital and analog. PRF is determined by 32K CLK, and all timings are connected with CLK_4m synchronous, completing four modes: 1 **sleep mode**, which configured by register SLEEP_EN, power consumption less than 2uA. 2 **data conversion mode**. 3 **PRF wait mode**.

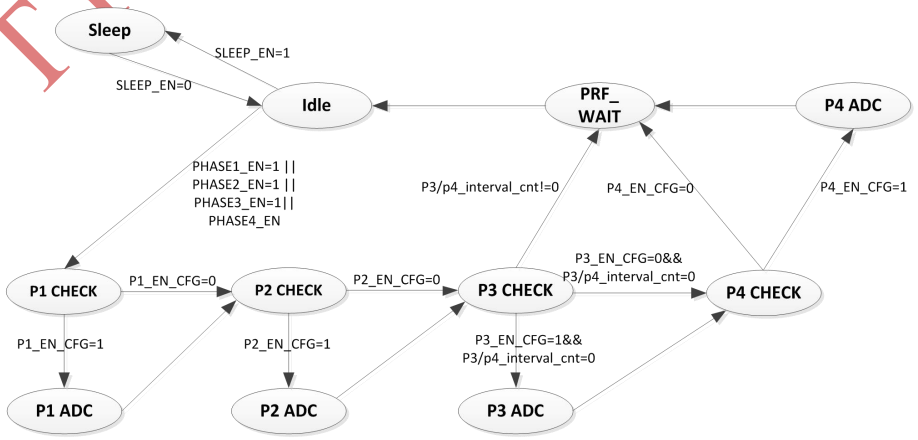

Figure 16. Chip State machine diagram(PPG)

SAR:

1 sleep mode: which is configured if no CH_EN is enabled. All the circuits except I2C and 32KHz OSC are shut down and the power consumption is less than 1uA.

2 scan mode: if any of the CH_NUM[1:0] is enabled,SAR will go to scan mode, in this mode the chip will periodically detect the capacitance on each sensor (if enabled). The scan period can be configured by register.

3 Doze mode: In some applications, the reaction/sensing time needs to be fast when the user is present (proximity detected), but can be slow when no detection has occurred for some time. If doze mode is enabled, the SAR will scan each channel (if enabled) by a relatively slow rate, and if user proximity is detected, it will accelerate the scan period and back to slow rate when proximity is released.

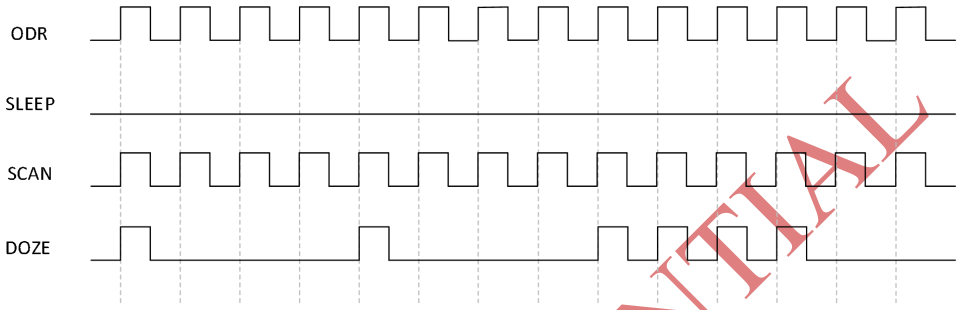

Figure 17 Working modes (SAR)

TIA or Integrator

The receiver input pins (INP, INN) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a transimpedance amplifier (TIA, when SW1 close) or a Integrator(when SW1 open), SW1 is set by register **0X60**. The TIA gain is set by its feedback resistor (Rf) and can be programmed through register **0x2C~0x2F**. The DC Offset IDAC current is used to cancellation DC part in signal. The signal chain is kept fully differential throughout the receiver channel in order to enable excellent rejection of common-mode noise as well as noise on power supplies.

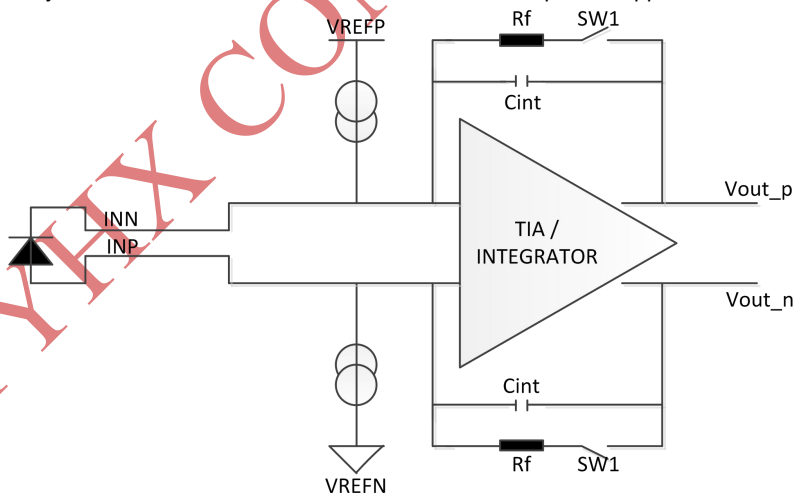

Figure 18. PPG signal Input circuit

TIA or Integrator Setting

TIA MODE : VOUT = Vout_P – Vout_N = 2×(I_signal – I_offset) ×Rf. The feedback resister register is **0x2C~0x2F;**

Offset IDAC

A typical optical heart-rate signal has a DC component and an AC component. Higher integrator gain can maximize the output AC signal. In order to eliminate the influence of DC level on the allowable AC signal gain, a current digital to analog converter (IDAC) is placed at the input of the device. By setting the programmable cancellation current (based on the DC current signal level), the effective signal obtained by the integrator can be reduced significantly. In each of the four phases of operation, the cancellation current is automatically presented to the input of the integrator. The ability to set different cancellation current in each of the four phases can be used to eliminate the ambient current in the ambient phase. During the LED on phase, this function can be used to offset the sum of ambient current and DC current of heart rate signal.

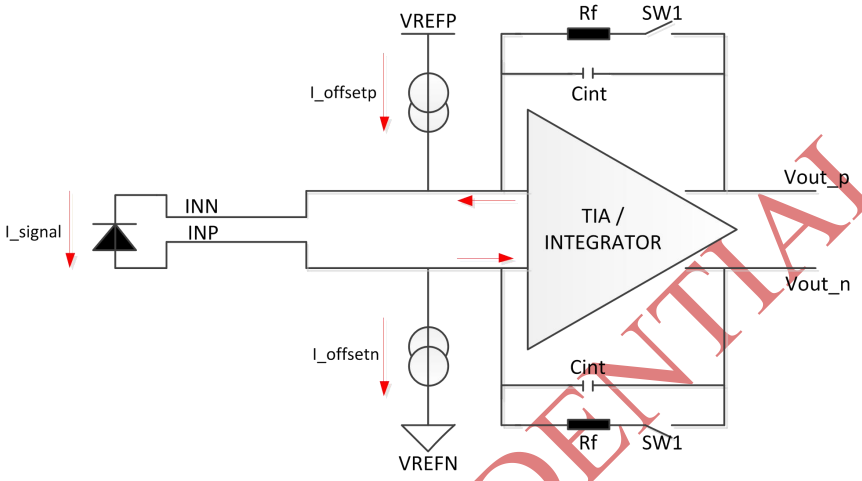

Figure 19. Offset IDAC

Offset Capacitance Compensation

The offset compensation scheme is used to compensate the capacitance of the sensor to the environment, i.e. PCB board. After the compensation, only the Cuser is feed into the ADC. HX9023E(M) can compensate up to 40pF parasitic cap. The offset cap calibration will be performed before the first measurement and after the calibration, the offset value will be stored into register for each channel.

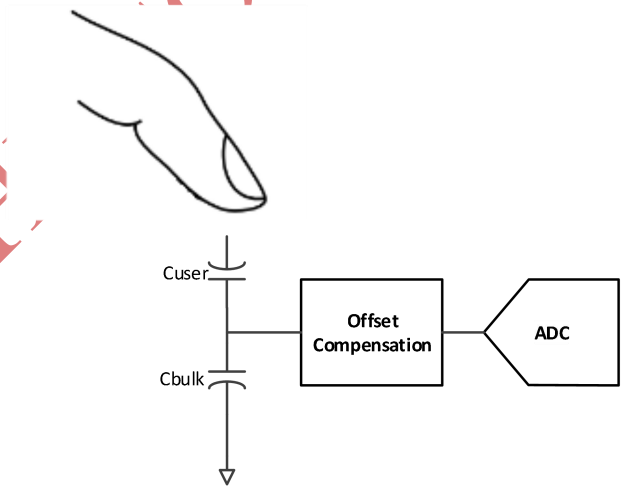

Figure20 Offset Compensation

LED Driver

The device has one internal current DAC with 8bits output current control. The DAC output current control though register **0x33** to **0x33** for phase1 to phase4.

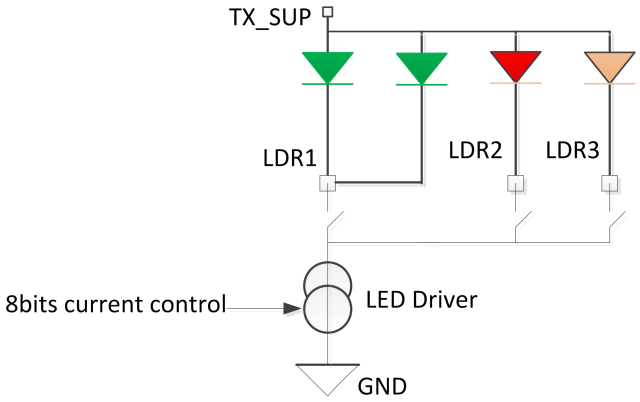

Figure 21. LED driver circuit

Digital Interface

I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address(PPG) is 0x44,the SAR part is 0x28. The register index will automatically increase by 1 after the addressed register has been accessed (read or write).And the format is shown as following:

A Acknowledge (0)

P Stop Condition

R Read (1)

S Start Condition

W Write (0)

Sr Repeated Start Condition

■ Master-to- Slave

□ Slave-to-Master

Figure22. I2C Data Format Diagram

I2C Electrical Characteristics

Table 2 Electrical Characteristics

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels (IO_SUP =1.8V)	VIL	0.5	0.54	n/a	n/a	V
			0.3 IO_SUP	0.5	0.3 IO_SUP	
HIGH level input voltage: fixed input levels (IO_SUP =1.8V)	VIH	1.26	n/a	1.26	n/a	V
		0.7 IO_SUP	Note(2)	0.7 IO_SUP	Note(2)	
Hysteresis of Schmitt trigger inputs: IO_SUP > 2 V	Vhys	n/a	n/a	0.05Vbus	–	V
IO_SUP < 2 V		n/a	n/a	0.1Vbus	–	
LOW level output voltage (open drain or open collector) at 3 mA sink current: IO_SUP > 2 V	VOL1	0	0.4	0	0.4	V
IO_SUP < 2 V	VOL2	n/a	n/a	0	0.2 IO_SUP	
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	–	250(4)	20+0.1 Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	-10(5)	10(5)	A
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1.Devices that use non-standard supply voltage switch don't conform to the intended I2C-bus system levels must relate input levels to the VDD voltage to which the pull-up resistors Rp are connected.

2.Maximum $V_{IH} = V_{DDmax} + 0.5V$.

3.C_b = capacitance of one bus line in pF.

4.The maximum tf for the SDA and SCL bus lines quoted in Table(300ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.

5.I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

n/a = not applicable

I2C Timing

The I2C Timing is as following figure:

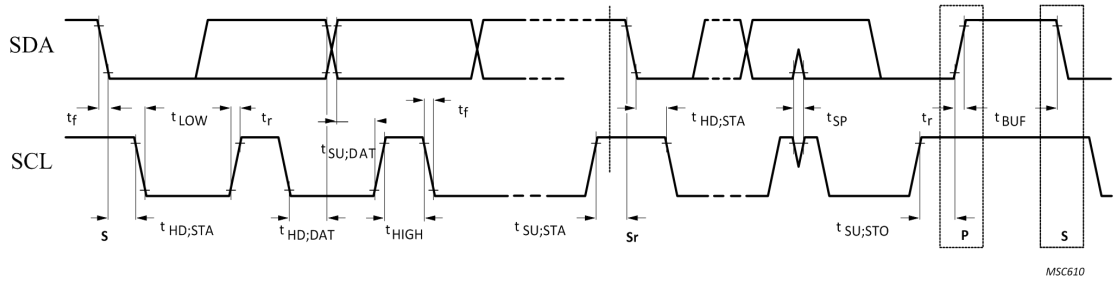

Figure 23. I²C Timing

Table 3 I²C Timing Parameters(1)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	us
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	us
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	us
Data hold time	tHD;DAT	0(2)	3.45(3)	0(2)	0.9(3)	us
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20+0.1Cb(5)	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20+0.1Cb(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	us
Capacitive load for each bus line	Cb	–	400	–	400	pF

Notes

1.All values referred to V_{IHmin} and V_{ILmax} levels (see Table2).

2.A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3.The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

4.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT≥250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

5.Cb=total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table2 are allowed.

Note： n/a = not applicable

Registers

Registers List

PPG

Address	Name	R/W	Function	Default
0x00	ID	RO	RA_PART_ID	0x69
0x01	REV_ID	RO	RA_REV_ID	0x22
0x02	SLEEP_EN	RW	Chip Sleep Function Enable	0x30
0x03	PHASE1_DATA	RO	Phase1_data [7:0]	0x00
0x04		RO	Phase1_data [15:8]	0x00
0x05		RO	Phase1_data [23:16]	0x00
0x06	PHASE3_DATA	RO	Phase3_data [7:0]	0x00
0x07		RO	Phase3_data [15:8]	0x00
0x08		RO	Phase3_data [23:16]	0x00
0x09	PHASE4_DATA	RO	Phase4_data [7:0]	0x00
0x0A		RO	Phase4_data [15:8]	0x00
0x0B		RO	Phase4_data [23:16]	0x00
0x0C	PHASE2_DATA	RO	Phase2_data [7:0]	0x00
0x0D		RO	Phase2_data [15:8]	0x00
0x0E		RO	Phase2_data [23:16]	0x00
0x0F	AFE_CFG1	RW	Data read lock configuration	0x00
0x12	FIFO_CFG1	RW	FIFO configuration Related	0x18
0x13	FIFO_CFG2	RW	FIFO configuration Related	0x32
0x14	FIFO_CFG3	RO	FIFO configuration Related	0x00
0x15	FIFO_DATA	RO	FIFO_Data_Out[7:0]	0x00
0x16		RO	FIFO_Data_Out [15:8]	0x00
0x17		RO	FIFO_Data_Out [23:16]	0x00
0x18	PHASE1/3_EN	RW	Phase1 and Phase3 enable and ADC OSR	0x33
0x19	PHASE2/4_EN	RW	Phase2 and Phase4 enable and ADC OSR	0x33
0x1A	PRF_CFG	RW	PRF cycle configuration [7:0]	0x00
0x1B		RW	PRF cycle configuration [15:8]	0x05
0x1C		RW	PRF cycle configuration [23:16]	0x00
0x1D	PHASE2/3	RW	Phase2/3_PRF_Interval	0x18
0x1E	AFE_TIMING1	RW	AFE_RST_cycle_sel	0x18
0x1F	AFE_TIMING2	RW	LED on time and enable phase select	0x3f
0x20	INT_CFG1	RW	INT configuration Related	0x03
0x21	INT_CFG2	RW	INT configuration Related	0x00
0x22	INT_CFG3	RW	INT configuration Related	0x00
0x23	INT_CFG4	RW	INT configuration Related	0x00
0x24	INT_CFG5	RW	INT configuration Related	0x01
0x25	INT_CFG6	RW	INT configuration Related	0x00
0x26	AFE_TIMING4	RW	Init_wait_delay_sel	0x0e
0x27	AFE_TIMING5	RW	Phase1/phase2 in PRF average	0x00
0x28	AFE_TIMING6	RW	Phase3/phase4 in PRF average	0x00
0x29	AFE_TIMING7	RW	Phase1/2/3/4 in PRF copy average	0x00
0x2C	PHASE1_RESCFG	RW	Phase1 TIA feedback resister configuration	0x04
0x2D	PHASE3_RESCFG	RW	Phase3 TIA feedback resister configuration	0x04
0x2E	PHASE4_RESCFG	RW	Phase4 TIA feedback resister configuration	0x04
0x2F	PHASE2_RESCFG	RW	Phase2 TIA feedback resister configuration	0x04
0x30	PHASE1_LEDDR	RW	Phase1 LED driver current configuration	0x80
0x31	PHASE3_LEDDR	RW	Phase3 LED driver current configuration	0x80
0x32	PHASE4_LEDDR	RW	Phase4 LED driver current configuration	0x80
0x33	PHASE2_LEDDR	RW	Phase2 LED driver current configuration	0x80
0x34	PHASE1_COMPONENTS_SEL	RW	Phase1 LED driver and external PD input	0x11
0x35	PHASE3_COMPONENTS_SEL	RW	Phase3 LED driver and external PD input	0x12
0x36	PHASE4_COMPONENTS_SEL	RW	Phase4 LED driver and external PD input	0x14

0x37	PHASE2_COMPONENTS_SEL	RW	Phase2 LED driver and external PD input	0x10
0x38	PHASE1_OFFSET_CFG	RW	Phase1 input offset IDAC configuration	0x00
0x39	PHASE3_OFFSET_CFG	RW	Phase3 input offset IDAC configuration	0x00
0x3A	PHASE4_OFFSET_CFG	RW	Phase4 input offset IDAC configuration	0x00
0x3B	PHASE2_OFFSET_CFG	RW	Phase2 input offset IDAC configuration	0x00
0x3C	PHASE1/3_AVG_CFG	RW	Phase1 and Phase3 average data number	0x00
0x3D	PHASE2/4_AVG_CFG	RW	Phase2 and Phase4 average data number	0x00
0x60	AFE _CFG1	RW	TIA and Integrator mode configuration and LED driver range configuration	0x8A
0x66	OFFSET_IDAC_CFG1	RW	Offset IDAC setting	0x91
0x69	RC_FLT_BP_EN	RW	RC filter bypass enable	0x30
0x6A	LOW_POWER_CFG	RW	Chip low power mode configuration	0x00

SAR

Address	Name	R/W	Function	Default
0x02	PRF_CFG	RW	PRF cycle configuration [4:0]	0x0B
0x03	CH0_CS_CFG	RW	Defines CH0 the connection of CS during conversion	0x0C
0x05	CH1_CS_CFG	RW	Defines CH1 the connection of CS during conversion	0x30
0x0D	RANGE_1_0	RW	Defines CH0 the full scale of conversion	0x00
0x10	RA_AVG0_NOSR0_CFG	RW	Defines the adc OSR of CH0	0x28
0x11	RA_NOSR12_CFG	RW	Defines the adc OSR of CH1	0x02
0x15	RA_OFFSET_DAC0_7_0	RW	Defines the offset capacitance during CH0	0x00
0x17	RA_OFFSET_DAC1_7_0	RW	Defines the offset capacitance during CH1	0x00
0x24	RA_CH_NUM_CFG	RW	Defines the phase en signal of [CH1, CH0]	0x00
0x38	RA_RAW_BL_RD_CFG	RW	Defines the output data of [CH1 CH0]	0x03
0x60	RA_DEVICE_ID	RW	DEVICE ID	0x15
0x6B	PROX_STATUS	RW	Indicates the proximity status of CH1 CH0	0x00
0x6F	RA_INT_WIDTH_CFG0	RW	Defines the Interrupt pulse width,	0x03
0x71	RA_INT_STATE_RD0	RW	Interrupt status	0x00
0x80	RA_PROX_HIGH_DIFF_CFG_CH0_0	RW	Defines the CH0 proximity high threshold	0x08
0x82	RA_PROX_HIGH_DIFF_CFG_CH1_0	RW	Defines the CH1 proximity high threshold	0x08
0xE9	RA_RAW_BL_CH0_1	RW	CH0 raw_data or baseline data[7:0]	0x00
0xEA	RA_RAW_DATA_CH0_2	RW	CH0 raw_data or baseline data[15:8]	0x00
0xEC	RA_RAW_BL_CH1_1	RW	CH1 raw_data or baseline data[7:0]	0x00
0xED	RA_RAW_DATA_CH1_2	RW	CH1 raw_data or baseline data[15:8]	0x00
0xF5	RA_LP_DIFF_CH0_1	RW	CH0 lp_data or diff data[7:0]	0x00
0xF6	RA_LP_DIFF_CH0_2	RW	CH0 lp_data or diff data[15:8]	0x00
0xF8	RA_LP_DIFF_CH1_1	RW	CH1 lp_data or diff data[7:0]	0x00
0xF9	RA_LP_DIFF_CH1_2	RW	CH1 lp_data or diff data[15:8]	0x00

Register Description

PPG

Register(0x00)

Address	Type	Default	Name	BIT	Default	Description
0x00	RO	0x69	Device_ID	7:0	69	HX3690Q chip ID

Register(0x01)

Address	Type	Default	Name	BIT	Default	Description
0x01	RO	0x22	Rev_ID	7:0	22	HX3690Q chip reversion ID

Register(0x02)

Address	Type	Default	Name	BIT	Default	Description
0x02	RW	0x30	Reserved	7:1	30	Reserved
			SLEEP_EN	0	0	1 : Power down 0 : Power on

Register(0x03,0x04,0x05)

Address	Type	Default	Name	BIT	Default	Description
0x03	RO	0x00	PS1_data1_out[7:0]	7:0	00	Phase1 data bits<7:0>
0x04	RO	0x00	PS1_data1_out[15:8]	15:8	00	Phase1 data bits<15:8>
0x05	RO	0x00	PS1_data1_out[19:16]	20:16	00	Phase1 data bits<20:16>

Register(0x06,0x07,0x08)

Address	Type	Default	Name	BIT	Default	Description
0x06	RO	0x00	PS3_data1_out[7:0]	7:0	00	Phase3 data bits<7:0>
0x07	RO	0x00	PS3_data1_out[15:8]	15:8	00	Phase3 data bits<15:8>
0x08	RO	0x00	PS3_data1_out[19:16]	20:16	00	Phase3 data bits<20:16>

Register(0x09,0x0A,0x0B)

Address	Type	Default	Name	BIT	Default	Description
0x09	RO	0x00	PS4_data1_out[7:0]	7:0	00	Phase4 data bits<7:0>
0x0A	RO	0x00	PS4_data1_out[15:8]	15:8	00	Phase4 data bits<15:8>
0x0B	RO	0x00	PS4_data1_out[19:16]	20:16	00	Phase4 data bits<20:16>

Register(0x0C,0x0D,0x0E)

Address	Type	Default	Name	BIT	Default	Description
0x0C	RO	0x00	PS2_data1_out[7:0]	7:0	00	Phase2 data bits<7:0>
0x0D	RO	0x00	PS2_data1_out[15:8]	15:8	00	Phase2 data bits<15:8>
0x0E	RO	0x00	PS2_data1_out[19:16]	20:16	00	Phase2 data bits<20:16>

Register(0x12)

Address	Type	Default	Name	BIT	Default	Description
0x12	RW	0x18	Reserved	7:6	0	Reserved
			FIFO watermark	5:0	18	Range 0~64 , used to set the number for FIFO almost full interrupt

Register(0x13)

Address	Type	Default	Name	BIT	Default	Description
0x13	RW	0x32	FIFO data sel	7:4	3	Select the data to store into the FIFO
			FIFO int clear mode sel	3:2	0	FIFO interrupt clear mode selection
			FIFO mode sel	1:0	2	FIFO work mode selection

Register(0x15,0x16,0x17)

Address	Type	Default	Name	BIT	Default	Description
0x15	RO	0x00	FIFO_data_out[7:0]	7:0	00	FIFO data bits<7:0>
0x16	RO	0x00	FIFO_data_out[15:8]	15:8	00	FIFO data bits<15:8>
0x17	RO	0x00	FIFO_data_out[23:16]	23:16	00	FIFO data bits<23:16>

Register(0x18)

Address	Type	Default	Name	BIT	Default	Description
0x18	RW	0x33	PS3_EN	7	0	Phase3 enable
			PS3 ADC OSR	6:4	3	Phase3 ADC over sample rate configuration
			PS1_EN	3	0	Phase1 enable
			PS1 ADC OSR	2:0	3	Phase1 ADC over sample rate configuration

Register(0x19)

Address	Type	Default	Name	BIT	Default	Description
0x19	RW	0x33	PS2_EN	7	0	Phase2 enable
			PS2 ADC OSR	6:4	3	Phase2 ADC over sample rate configuration
			PS4_EN	3	0	Phase4 enable
			PS4 ADC OSR	2:0	3	Phase4 ADC over sample rate configuration

Register(0x1A,0x1B,0x1C)

Address	Type	Default	Name	BIT	Default	Description
0x1A	RW	0x00	PRF [7:0]	7:0	00	PRF configuration bits<7:0>
0x1B	RW	0x05	PRF [15:8]	15:8	05	PRF configuration bits<15:8>
0x1C	RW	0x00	PRF [23:16]	23:16	00	PRF configuration bits<23:16>

Register(0x1D)

Address	Type	Default	Name	BIT	Default	Description
0x1D	RW	0x18	PS3/4 INTERVAL	7:0	18	Phase3/4 conversion interval of PRF

Register(0x1E)

Address	Type	Default	Name	BIT	Default	Description
0x1E	RW	0x18	Reserved	7:6	0	Reserved
			TIA_RESET_CLK	5:3	3	AFE_RST width
			Reserved	2:0	0	Reserved

Register(0x1F)

Address	Type	Default	Name	BIT	Default	Description
0x1F	RW	0x3f	Reserved	7	0	Reserved
	RW		LED_ON	6:4	3	LED on time configuration
	RW		PS1 LED EN	3	1	Phase1 LED driver enable
	RW		PS3 LED EN	2	1	Phase3 LED driver enable
	RW		PS4 LED EN	1	1	Phase4 LED driver enable
	RW		PS2 LED EN	0	1	Phase2 LED driver enable

Register(0x20)

Address	Type	Default	Name	BIT	Default	Description
0x20	RW	0x03	Rddata_clr_all_int_en	7	0	The selection of clear interrupt
	RW		Int_width	6:0	3	Set pulse width of the INT_N pin

Register(0x21)

Address	Type	Default	Name	BIT	Default	Description
0x21	RO	0x00	PS1_data_rdy_int	7	0	PS1 conversion interrupt
	RO		PS3_data_rdy_int	6	0	PS3 conversion interrupt
	RO		PS4_data_rdy_int	5	0	PS4 conversion interrupt
	RO		PS2_data_rdy_int	4	0	PS2 conversion interrupt
	RO		Reserve	3:0	0	Reserve

Register(0x22)

Address	Type	Default	Name	BIT	Default	Description
0x22	RO	0x00	Full_int	7	0	Fifo full interrupt
	RO		Empty_int	6	0	Empty_int interrupt
	RO		Almost_full_int	5	0	Almost_full_int interrupt
	RO		Overflow_int	4	0	Overflow_int interrupt
	RO		Underflow_int	3	0	Underflow_int interrupt
	RO		Stream_drop_int	2	0	Stream_drop_int interrupt
	RO		I2c_rd_timeout_int	1	0	I2c_rd_timeout_int interrupt
	RO		Prf_cnt_over_int	0	0	Prf_cnt_over interrupt

Register(0x23)

Address	Type	Default	Name	BIT	Default	Description
0x23	RW	0x00	PS1_data_rdy_int_en	7	0	PS1 conversion interrupt enalbe
	RW		PS3_data_rdy_int_en	6	0	PS3 conversion interrupt enalbe
	RW		PS4_data_rdy_int_en	5	0	PS4 conversion interrupt enalbe
	RW		PS2_data_rdy_int_en	4	0	PS2 conversion interrupt enalbe
	RW		Reserve	3:0	0	Reserve

Register(0x24)

Address	Type	Default	Name	BIT	Default	Description
0x24	RO	0x00	Full_int_en	7	0	Fifo full interrupt enalbe
	RO		Empty_int_en	6	0	Empty_int interrupt enalbe
	RO		Almost_full_int_en	5	0	Almost_full_int interrupt enalbe
	RO		Overflow_int_en	4	0	Overflow_int interrupt enalbe
	RO		Underflow_int_en	3	0	Underflow_int interrupt enalbe
	RO		Stream_drop_int_en	2	0	Stream_drop_int interrupt enalbe
	RO		I2c_rd_timeout_int_en	1	0	I2c_rd_timeout_int interrupt enalbe
	RO		Prf_cnt_over_int_en	0	0	Prf_cnt_over interrupt enalbe

Register(0x25)

Address	Type	Default	Name	BIT	Default	Description
0x25	RW	0x00	PS1_int_clr_mode_i2c	7:6	0	Clear mode of phase1 interrupt
	RW		PS3_int_clr_mode_i2c	5:4	0	Clear mode of phase3 interrupt
	RW		PS4_int_clr_mode_i2c	3:2	0	Clear mode of phase4 interrupt
	RW		PS2_int_clr_mode_i2c	1:0	0	Clear mode of phase3 interrupt

Register(0x26)

Address	Type	Default	Name	BIT	Default	Description
0x26	RW	0x0e	Reserved	7	0	Reserved
	RW		Init_wait_delay_sel	6:4	0	Settle time before PS1 conversion
	RW		PS1_offset_idac_en	3	1	Phase1 offset idac enable
	RW		PS3_offset_idac_en	2	1	Phase3 offset idac enable
	RW		PS4_offset_idac_en	1	1	Phase4 offset idac enable
	RW		PS2_offset_idac_en	0	1	Phase2 offset idac enable

Register(0x27)

Address	Type	Default	Name	BIT	Default	Description
0x27	RO	0x00	Reserved	7	0	Reserved
	RW		PS2_inner_avg_sel_i2c	6:4	0	Phase2 in prf inner average select
	RW		Reserved	3	0	Reserved
	RW		PS1_inner_avg_sel_i2c	2:0	0	Phase1 in prf inner average select

Register(0x28)

Address	Type	Default	Name	BIT	Default	Description
0x28	RO	0x00	Reserved	7	0	Reserved
	RW		PS4_inner_avg_sel_i2c	6:4	0	Phase4 in prf inner average select
	RW		Reserved	3	0	Reserved
	RW		PS3_inner_avg_sel_i2c	2:0	0	Phase3 in prf inner average select

Register(0x29)

Address	Type	Default	Name	BIT	Default	Description
0x29	RW	0x00	CIC_EN	7	0	Digital filter CIC mode enable
	RW		CIC_BITS2_EN	6	0	Digital filter CIC mode count from bits2 enable
	RW		PPG_samp_delay_sel_i2c	5:4	0	Led en to sample en delay in 4M clk number
	RW		Reserved	3	0	Reserved
	RW		Outer_avg_num_sel_i2c	2:0	0	Phase 1/2/3/4 in prf copy average time

Register(0x2C)

Address	Type	Default	Name	BIT	Default	Description
0x2C	RO	0x04	Reserved	7:3	0	Reserved
	RW		PS1_TIA_RES	2:0	4	Phase1 TIA resister configuration

Register(0x2D)

Address	Type	Default	Name	BIT	Default	Description
0x2D	RO	0x04	Reserved	7:3	0	Reserved
	RW		PS3_TIA_RES	2:0	4	Phase3 TIA resister configuration

Register(0x2E)

Address	Type	Default	Name	BIT	Default	Description
0x2E	RO	0x04	Reserved	7:3	0	Reserved
	RW		PS4_TIA_RES	2:0	4	Phase4 TIA resister configuration

Register(0x2F)

Address	Type	Default	Name	BIT	Default	Description
0x2F	RO	0x04	Reserved	7:3	0	Reserved
	RW		PS2_TIA_RES	2:0	4	Phase2 TIA resister configuration

Register(0x30)

Address	Type	Default	Name	BIT	Default	Description
0x30	RW	0x80	PS1_leddr_cfg	7:0	80	Phase1 LED driver current

Register(0x31)

Address	Type	Default	Name	BIT	Default	Description
0x31	RW	0x80	PS3_leddr_cfg	7:0	80	Phase3 LED driver current

Register(0x32)

Address	Type	Default	Name	BIT	Default	Description
0x32	RW	0x80	PS4_leddr_cfg	7:0	80	Phase4 LED driver current

Register(0x33)

Address	Type	Default	Name	BIT	Default	Description
0x33	RW	0x80	PS2_leddr_cfg	7:0	80	Phase2 LED driver current

Register(0x34)

Address	Type	Default	Name	BIT	Default	Description
0x34	RW	0x11	Reserved	7	0	Reserved
	RW		PS1_input_sel	6:4	1	Phase1 external PD select
	RW		PS1_LDR_sel	3:0	1	Phase1 LED driver select

Register(0x35)

Address	Type	Default	Name	BIT	Default	Description
0x35	RW	0x12	Reserved	7	0	Reserved
	RW		PS3_input_sel	6:4	1	Phase3 external PD select
	RW		PS3_LDR_sel	3:0	1	Phase3 LED driver select

Register(0x36)

Address	Type	Default	Name	BIT	Default	Description
0x36	RW	0x14	Reserved	7	0	Reserved
	RW		PS4_input_sel	6:4	1	Phase4 external PD select
	RW		PS4_LDR_sel	3:0	1	Phase4 LED driver select

Register(0x37)

Address	Type	Default	Name	BIT	Default	Description
0x37	RW	0x10	Reserved	7	0	Reserved
	RW		PS2_input_sel	6:4	1	Phase2 external PD select
	RW		PS2_LDR_sel	3:0	1	Phase2 LED driver select

Register(0x38)

Address	Type	Default	Name	BIT	Default	Description
0x38	RW	0x00	Reserved	7	0	Reserved
	RW		PS1_offset_idac_cfg	6:0	0	Phase1 Offset IDAC configuration

Register(0x39)

Address	Type	Default	Name	BIT	Default	Description
0x39	RW	0x00	Reserved	7	0	Reserved
	RW		PS3_offset_idac_cfg	6:0	0	Phase3 Offset IDAC configuration

Register(0x3A)

Address	Type	Default	Name	BIT	Default	Description
0x3A	RW	0x00	Reserved	7	0	Reserved
	RW		PS4_offset_idac_cfg	6:0	0	Phase4 Offset IDAC configuration

Register(0x3B)

Address	Type	Default	Name	BIT	Default	Description
0x3B	RW	0x00	Reserved	7	0	Reserved
	RW		PS2_offset_idac_cfg	6:0	0	Phase2 Offset IDAC configuration

Register(0x3C)

Address	Type	Default	Name	BIT	Default	Description
0x3C	RW	0x00	Reserved	7	0	Reserved
	RW		PS1_AVERAGE_ADC_OUT	6:4	0	Phase1 ADC average output
	RW		Reserved	4	0	Reserved
	RW		PS3_AVERAGE_ADC_OUT	3:0	0	Phase3 ADC average output

Register(0x3D)

Address	Type	Default	Name	BIT	Default	Description
0x3D	RW	0x00	Reserved	7	0	Reserved
	RW		PS4_AVERAGE_ADC_OUT	6:4	0	Phase4 ADC average output
	RW		Reserved	4	0	Reserved
	RW		PS2_AVERAGE_ADC_OUT	3:0	0	Phase2 ADC average output

Register(0x60)

Address	Type	Default	Name	BIT	Default	Description
0x60	RW	0x8a	Reserved	7:6	2	Reserved
	RW		Reserved	5:4	0	Reserved
	RW		Reserved	3:2	2	Reserved
	RW		TIA_INTEGRATOR	1	1	TIA or integrator mode configuration

Register(0x66)

Address	Type	Default	Name	BIT	Default	Description
0x66	RW	0x91	Reserved	7:4	0	Reserved
	RW		OFFSET_IDAC_POL	3	0	Offset idac output polarity select
	RW		Reserved	2	0	Reserved
	RW		OFFSET_IDAC1_EN	1	1	Offset IDAC1 enable range 0~32uA
	RW		OFFSET_IDAC2_EN	0	0	Offset IDAC2 enable range 0~32uA

Register(0x6A)

Address	Type	Default	Name	BIT	Default	Description
0x6A	RW	0x00	Reserved	7:2	0	Reserved
	RW		Low power enable	1	0	Low power mode enable
	RW		Reserved	0	0	Reserved

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Register(0x02)

Address	Type	Default	Name	BIT	Default	Description
0x02	RW	0x0b	PRF_CFG	4:0	0b	PRF configuration

Register(0x03)

Address	Type	Default	Name	BIT	Default	Description
0x03	RW	0x0c	CH0_CFG_7_0	5:0	0c	Configure CH0 the connection of CS

Register(0x05)

Address	Type	Default	Name	BIT	Default	Description
0x05	RW	0x30	CH1_CFG_7_0	5:0	30	Configure CH1 the connection of CS

Register(0x0D)

Address	Type	Default	Name	BIT	Default	Description
0x0D	RW	0x00	Range_i2c_CH1	3:2	0	Defines CH1 the full scale
	RW		Range_i2c_CH0	1:0	0	Defines CH0 the full scale

Register(0x10)

Address	Type	Default	Name	BIT	Default	Description
0x10	RW	0x28	CH0_AVG_num_i2c	7:5	2	Defines the adc avg number of CH0
	RW		OSR0_num_i2c	3:2	8	Defines the adc OSR of CH0

Register(0x11)

Address	Type	Default	Name	BIT	Default	Description
0x11	RW	0x02	Reserved	7:3	0	Reserved
	RW		OSR0_num_i2c	2:0	2	Defines the adc OSR of CH1

Register(0x15,0x16)

Address	Type	Default	Name	BIT	Default	Description
0x15	RW	0x00	offset_dac0_i2c[7:0]	7:0	0	Defines CH0 offset capacitance[7:0]
0x16	RW	0x00	offset_dac0_i2c[9:8]	9:8	0	Defines CH0 offset capacitance[9:8]

Register(0x17,0x18)

Address	Type	Default	Name	BIT	Default	Description
0x17	RW	0x00	offset_dac1_i2c[7:0]	7:0	0	Defines CH1 offset capacitance[7:0]
0x18	RW	0x00	offset_dac1_i2c[9:8]	9:8	0	Defines CH1 offset capacitance[9:8]

Register(0x24)

Address	Type	Default	Name	BIT	Default	Description
0x24	RW	0x00	Reserved	7:2	0	Reserved
	RW		CH_num_i2c	1:0	0	Defines the en signal of [CH1, CH0]

Register(0x38)

Address	Type	Default	Name	BIT	Default	Description
0x38	RW	0x03	Raw_bl_sel	5:4	0	Select raw_data or bl_data
	RW		LP_diff_sel	1:0	0	Select lp_data or diff_data

Register(0x60)

Address	Type	Default	Name	BIT	Default	Description
0x60	RW	0x15	RA_Device_ID	7:0	15	Device ID

Register(0x6B)

Address	Type	Default	Name	BIT	Default	Description
0x6B	RW	0x00	Reserved	7:4	00	Reserved
	RW		RA_prox_status	1:0	00	Indicates the proximity occurrence

Register(0x6F)

Address	Type	Default	Name	BIT	Default	Description
0x6F	RW	0x03	Reserved	7:4	0	Reserved
	RW		INT_width_sel_i2c	2:0	3	Defines the Interrupt pulse width

Register(0x80,0x82)

Address	Type	Default	Name	BIT	Default	Description
0x80	RW	0x08	Prox_high_diff_CFG0_i2c	7:4	0	Defines CH0 proximity high threshold
0x82	RW	0x08	Prox_high_diff_CFG1_i2c	2:0	3	Defines CH1 proximity high threshold

Register(0xE9,0xEA)

Address	Type	Default	Name	BIT	Default	Description
0xE9	RO	0x00	Raw_data_CH0[7:0]	7:0	0	CH0 raw_data or baseline data[7:0]
0xEA	RO	0x00	Raw_data_CH0[15:8]	7:0	0	CH0 raw_data or baseline data[15:8]

Register(0xEC,0xED)

Address	Type	Default	Name	BIT	Default	Description
0xEC	RO	0x00	Raw_data_CH1[7:0]	7:0	0	CH1 raw_data or baseline data[7:0]
0xED	RO	0x00	Raw_data_CH1[15:8]	7:0	0	CH1 raw_data or baseline data[15:8]

Register(0xF5,0xF6)

Address	Type	Default	Name	BIT	Default	Description
0xF5	RO	0x00	LP_out_CH0[7:0]	7:0	0	CH0 lp_data or diff data[7:0]
0xF6	RO	0x00	LP_out_CH0[15:8]	7:0	0	CH0 lp_data or diff data[15:8]

Register(0xF8,0xF9)

Address	Type	Default	Name	BIT	Default	Description
0xF8	RO	0x00	LP_out_CH1[7:0]	7:0	0	CH1 lp_data or diff data[7:0]
0xF9	RO	0x00	LP_out_CH1[15:8]	7:0	0	CH1 lp_data or diff data[15:8]

Application Information

Reference Schematic

A typical I2C interface application Schematic Diagram and Typical SPI Interface Application Schematic Diagram for HX3690S is shown in Figure 24. The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistor (Rp). It is recommended use 10 kΩ resistor when running at 400kbps.

DEVICE NAME	Value	Description
LDO_PPG	2.7~3.6 V	Low noise
LDO_SAR	1.8V	Low noise
R0,R5,R6	0 Ω	
R1,R2,R3,R4	10 K Ω	
C0	4.7 uF	
C1,C4	1 uF	
C3	10 uF	
C2	100nF	
C5	10pF	
C6	5pF	

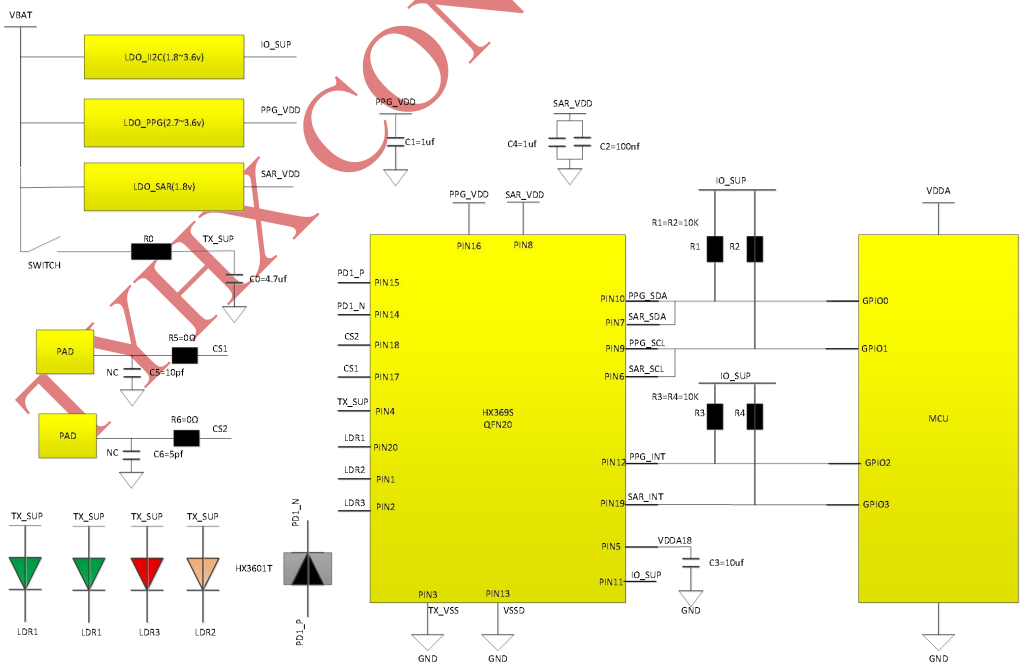
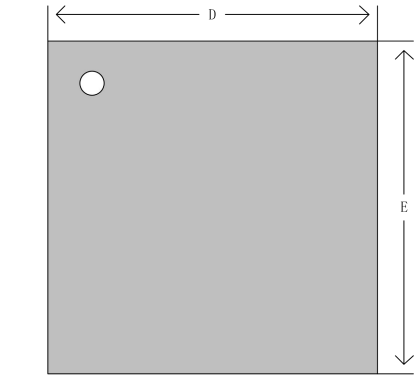


Figure 24 Typical I2C Interface Application Schematic Diagram

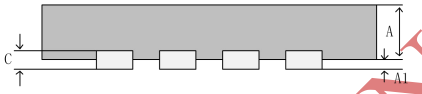
Notes: When the chip is powered off（PPG_VDD=0V）, the SWITCH must be turned off

Package Information

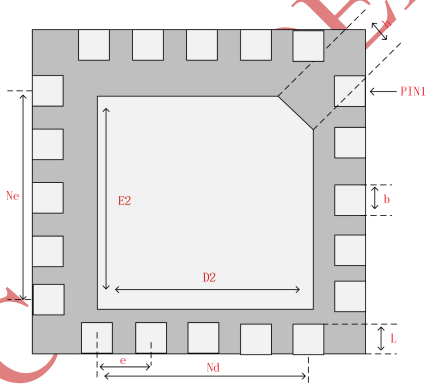
Mechanical Dimension



TOP VIEW



SIDE VIEW



Bottom View

SYMBOL	MILLIMETER		
	MIN	MON	MAX
A	0.65	0.75	0.85
A1		0.02	0.05
b	0.16	0.2	0.24
c	0.18	0.2	0.25
D	2.9	3	3.1
D2	1.6	1.7	1.8
e	0.4BSC		
Ne	1.6BSC		
Nd	1.6BSC		
E	2.9	3	3.1
E2	1.6	1.7	1.8
L	0.25	0.3	0.35
h	0.2	0.25	0.3

Recommended PCB Pad Layout

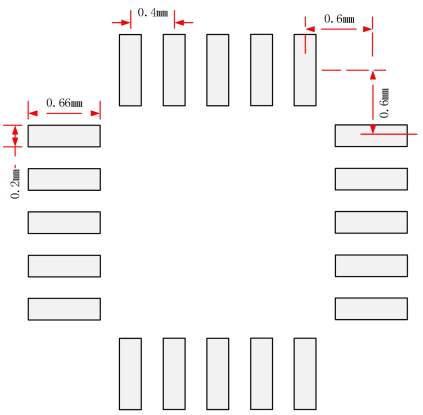


Figure 25. Mounting layout

Soldering Information

HX3690S has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment and materials used in these test are detailed below. The reflow soldering profile describes the expect maximum heat exposure of components during the reflow soldering process. Temperature is measured on top of components. The soldering process should be limited to a maximum of three phases according to this reflow soldering profile.

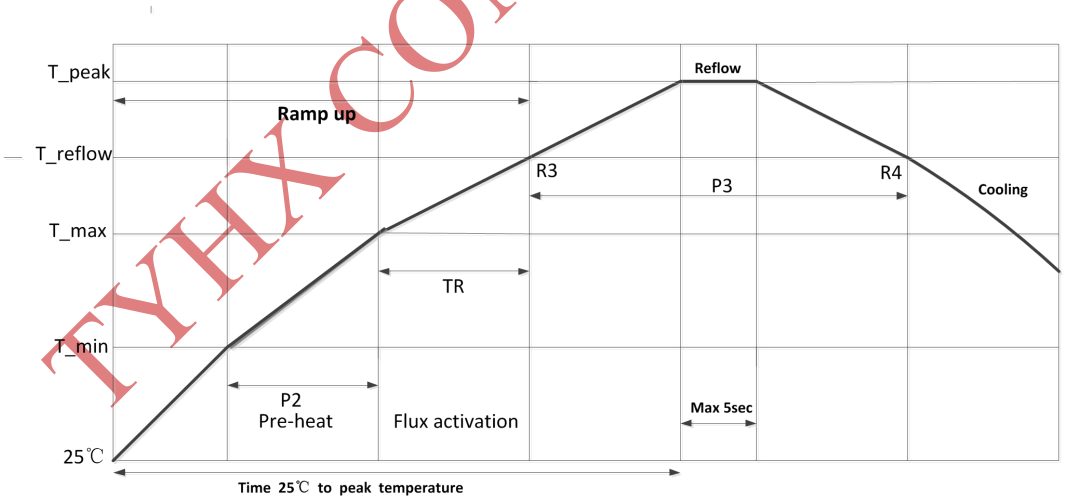


Figure26. HX3690S Reflow Profile Graph

The detail parameters are listed in the following table:

Table 4 Reflow Soldering Profile Parameters

	Peak temperature (Tpeak)	250℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃； 100S to 180S
	P2：（T min to max）	90-110s
Time maintain above	Temperature (Treflow)	217 ℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

Carrier Drawing

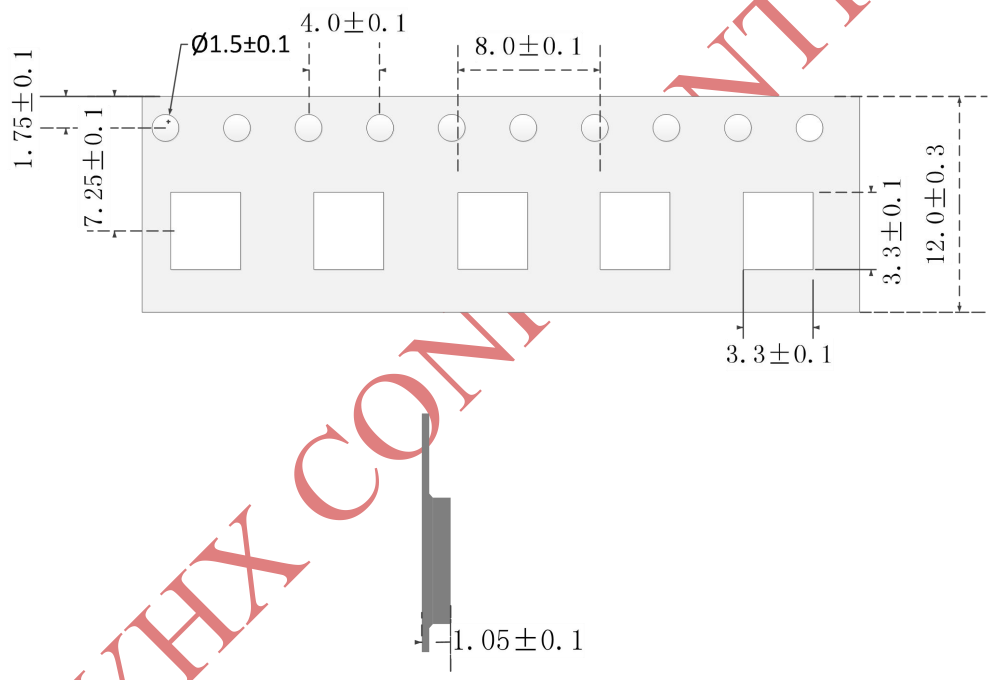


Figure 27. Carrier Drawing

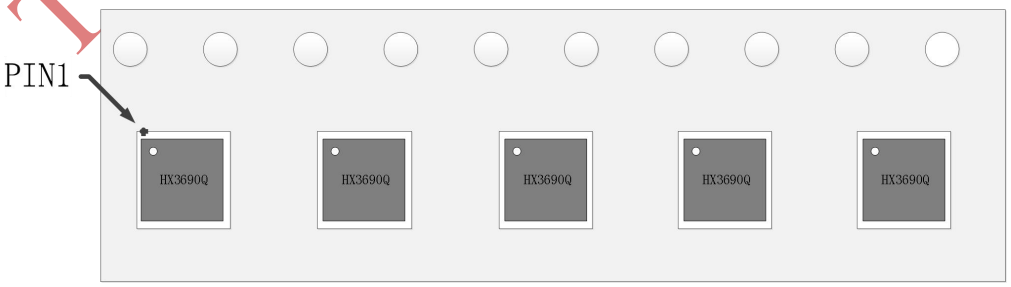


Figure 28. Unit Orientation

The Maximum capacity of one packing box:One lnner packing box = 1000PCS

Note:The Tape and Reel packing with vacuum pack is 1 year storage available @25℃， 50%RH。